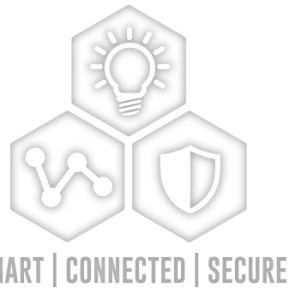
30 kW 3-Phase Vienna PFC and PLECS Simulation Model

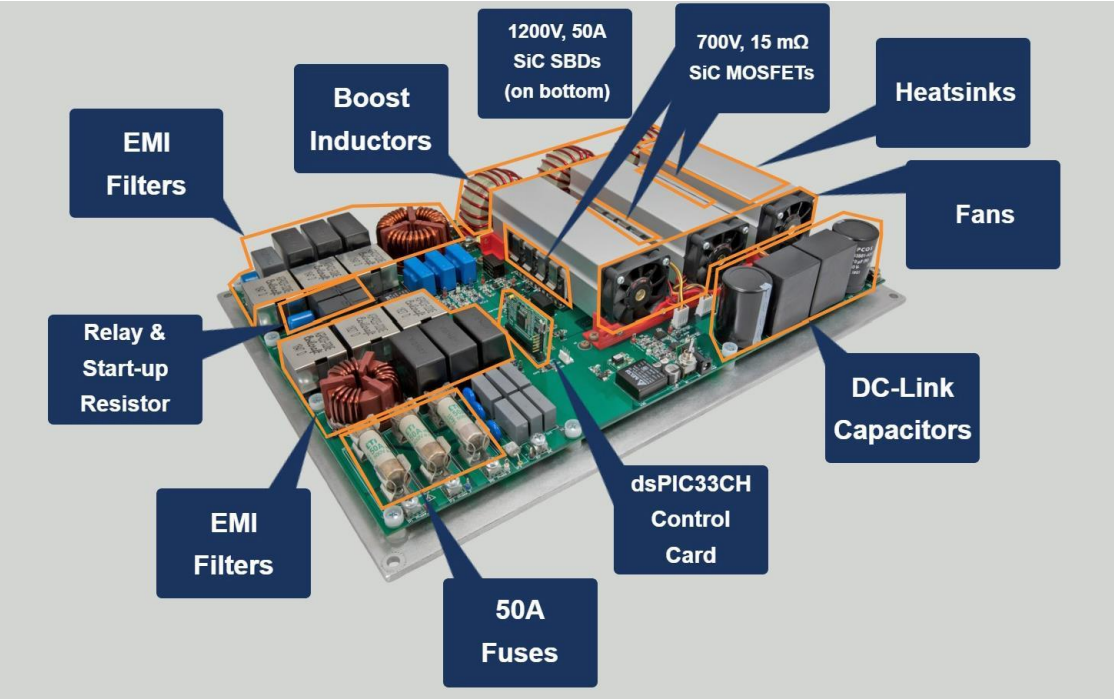
A Leading Provider of Smart, Connected and Secure Embedded Solutions



Discrete and Power Management

December 2021

Vienna PFC Reference Design Overview



MSCSICPFC/REF5 (www.microchip.com/PFC)

- Design files, dsPIC33CH code, and User's Guide
- SiC device SPICE models available at microchip.com/sic
- PLECS model with Quick Start Guide
- Hardware not included

- 30 kW Vienna rectifier topology with 98.6 % peak efficiency
- 3-phase 380/400 V, 50/60 Hz AC input with 700 V DC output voltage
- Design for 20 % over voltage on the line
- Microchip 700 V SiC MOSFETs and 1200 V SiC Schottky Barrier Diodes (SBD)
- 140 kHz PWM switching frequency
- dsPIC® DSC 3-level modulation digital control
- < 5 % current THD at half and full loads
- PCB design according to IEC standards, with consideration for safety, current stress, mechanical stress and noise immunity
- IEEE Publication
  - S. Chen, W. Yu, D. Meyer, "Design and Implementation of Forced Air-cooled, 140kHz, 20kW SiC MOSFET based Vienna PFC"
- Video Overview
  - "APEC 2019: Here's How to Build an EV Charger with SiC Transistors" (https://www.youtube.com/watch?v=pBTqJI-4pKA)

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Vienna PFC Reference Design

Hardware Overview

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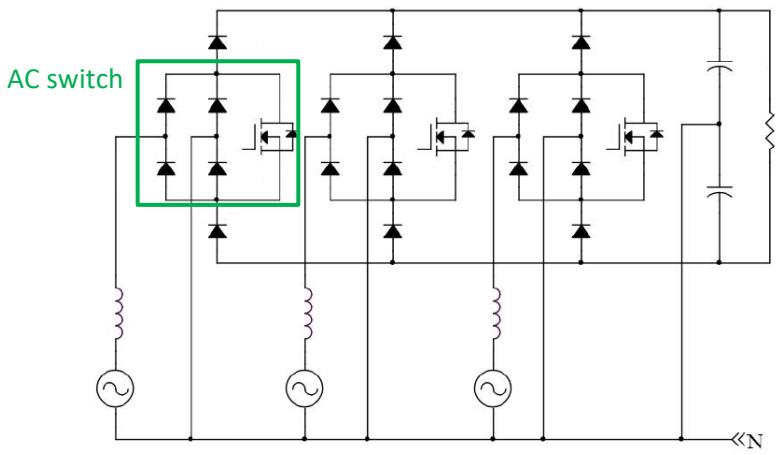
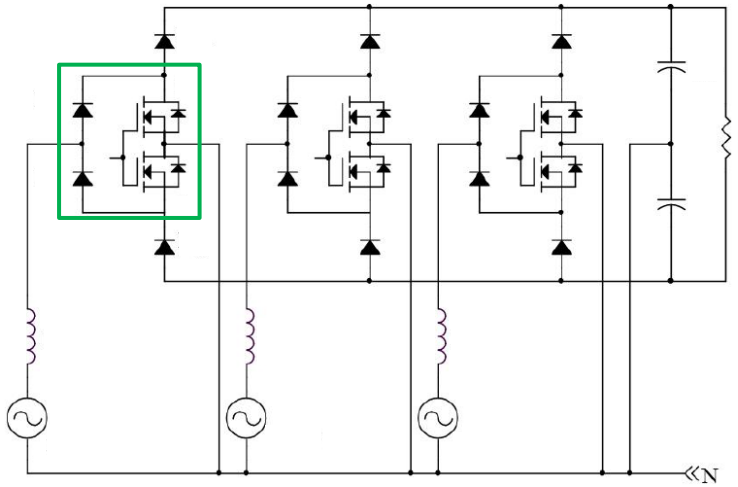
Vienna Rectifier Topologies

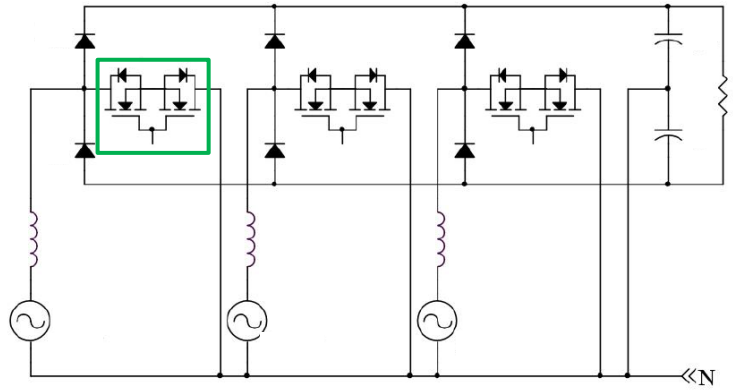
Topology I
Classical Version



Topology II



Topology III
Reference Design (3-wire)



- **3-Level Modulation**
  - Neutral, when MOSFET is on
  - ½ V_{DC} output, when upper FWD is on
  - -½ V_{DC} output, when lower FWD is on

- **Reference:**

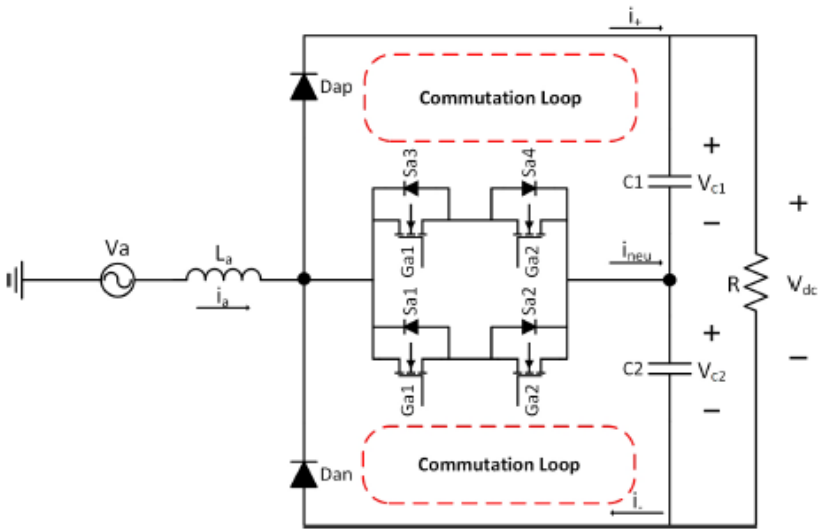
Thesis - Anna University

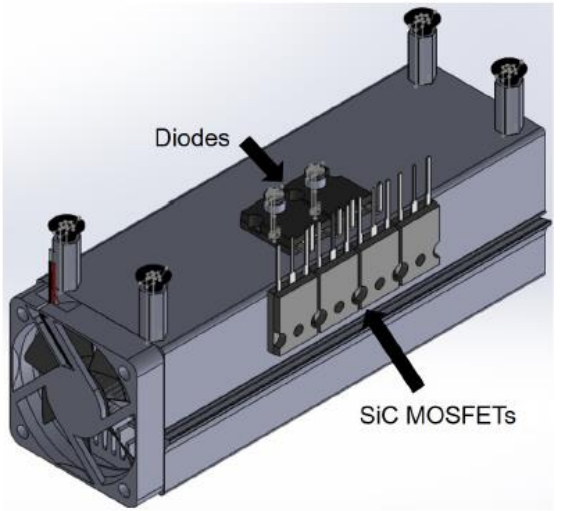
- **Topology I**
  - **Pro's:** single MOSFET per phase, low-cost Si diodes, easy to control
  - **Con's:** MOSFET losses significant
- **Topology II**
  - **Pro's:** two MOSFETs per phase, fewer diodes, easy to control, lower MOSFET losses (on only for half-wave)
  - **Con's:** lower power density than topology III
- **Topology III**
  - **Pro's:** two MOSFETs per phase, no Si diodes, lower MOSFET losses over topology I (no switching losses for one half-wave), fewest components resulting in highest power density
  - **Con's:** difficult to control

Double-Sided Assembly

- **Commutation loop inductance can potentially cause high overshoot voltage on the drain and higher switching loss, resulting in lower efficiency**

- **Reference Design overcomes this issue by using a two-sided arrangement, resulting in 25% reduction in the commutation loop over a single-row arrangement (figures from IEEE paper)**





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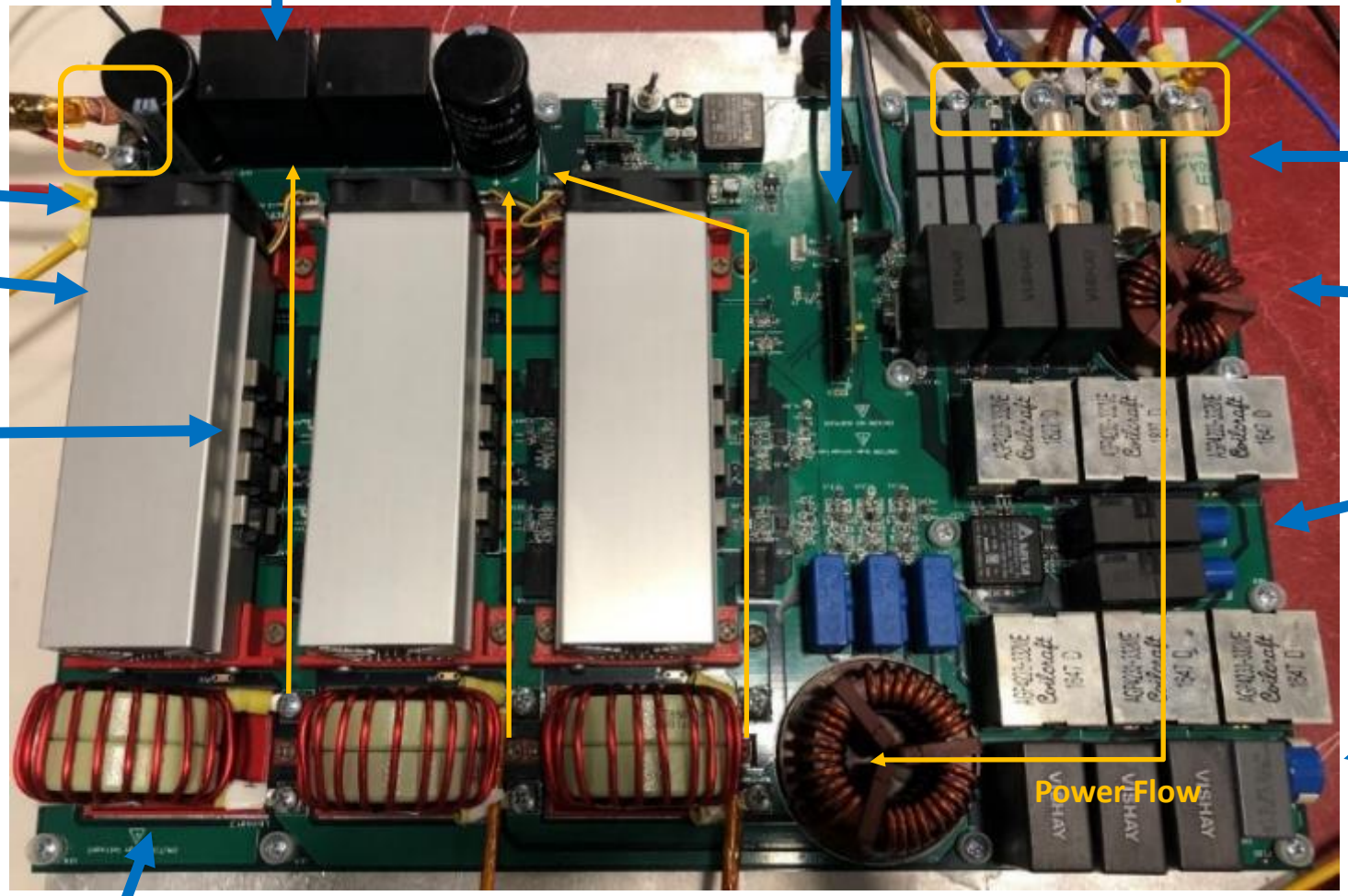
PCB Assembly



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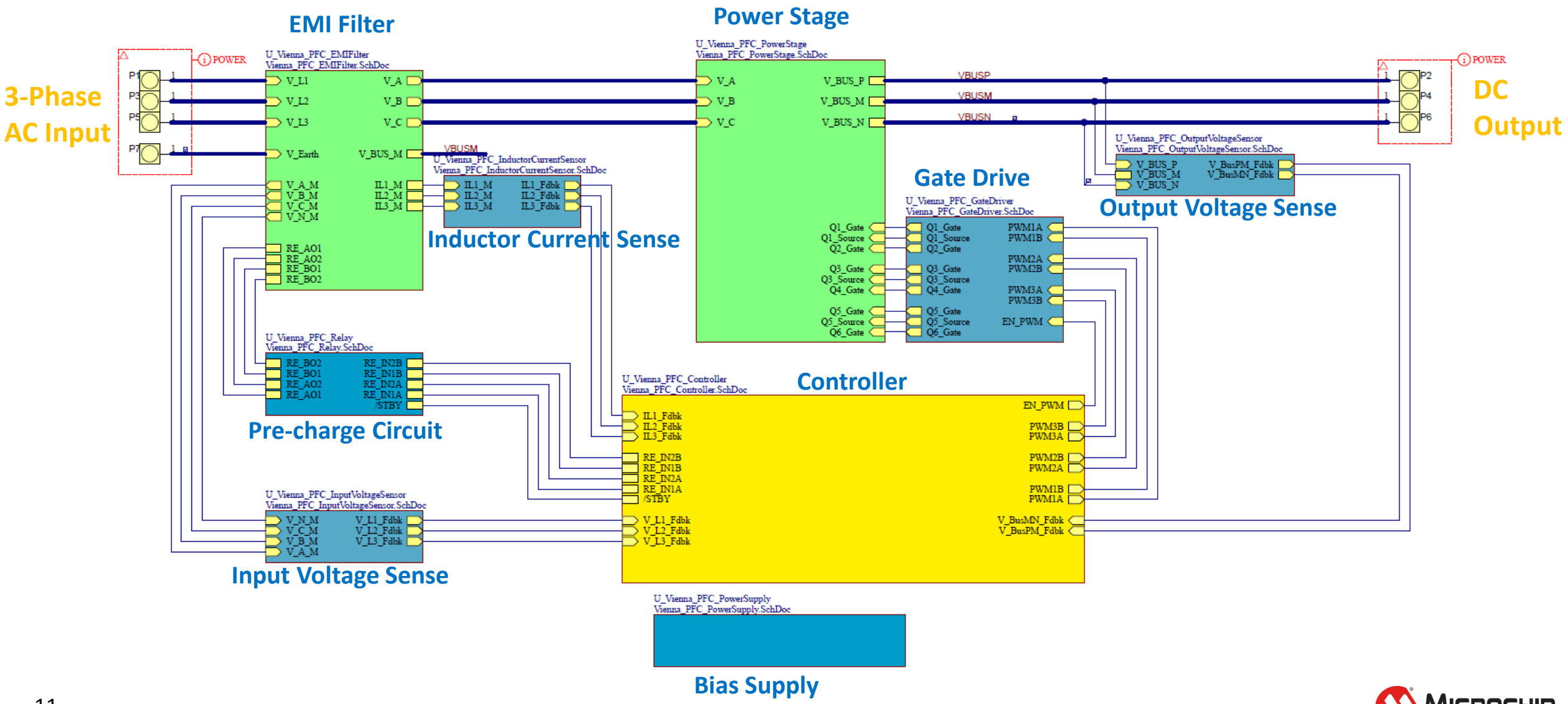
Top-Level Schematic



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Lab Setup

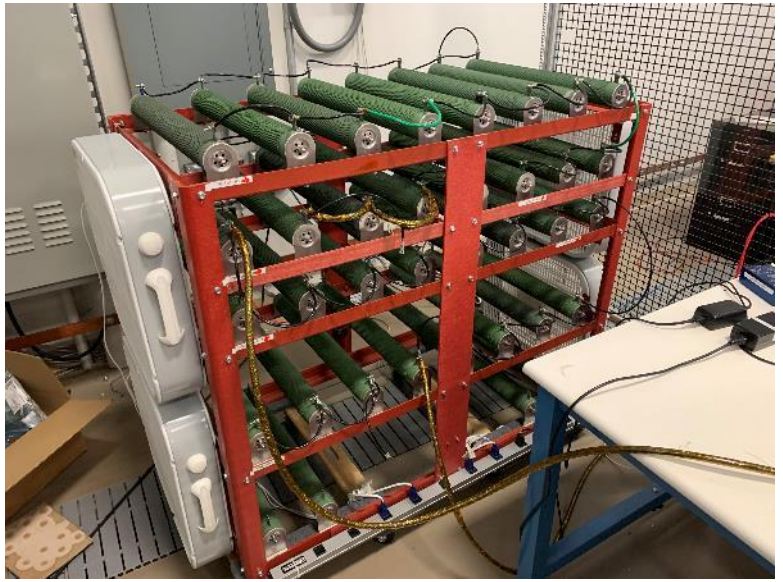
- **30 kW test capability**
- **Equipment**
  - 30 kW 3-Phase AC source (California Instruments MX30)
  - Passive load bank (>>30 kW)
  - Power meter (Yokogawa WT3000)

Power Meter

AC Source

Test Bench

Passive Load Bank



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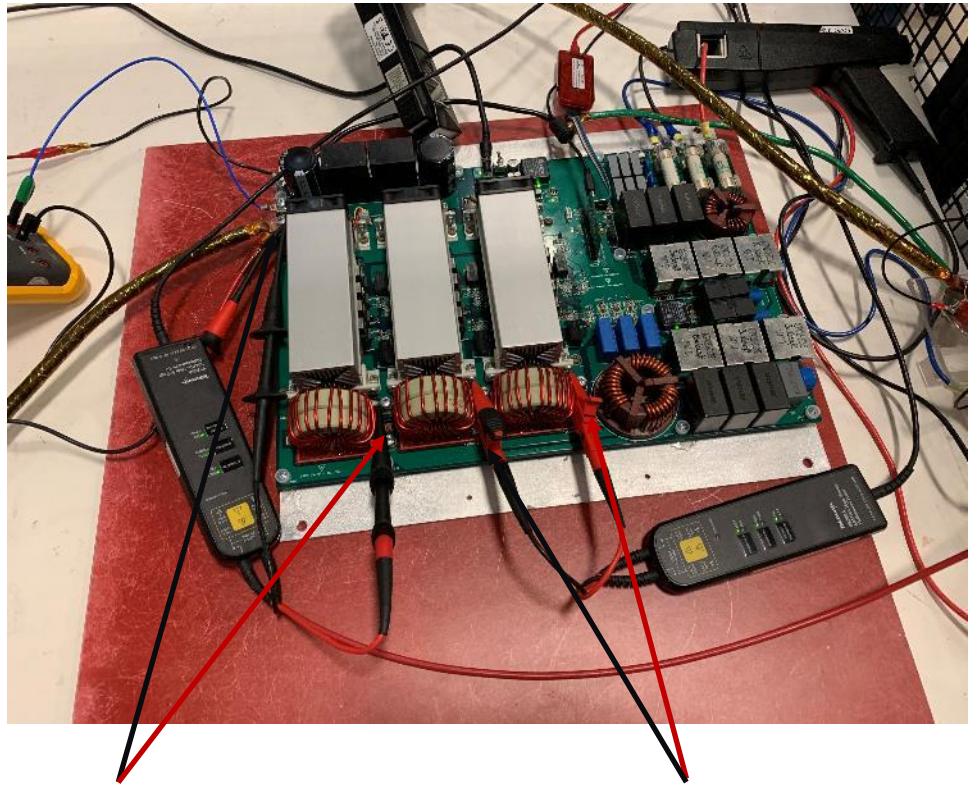
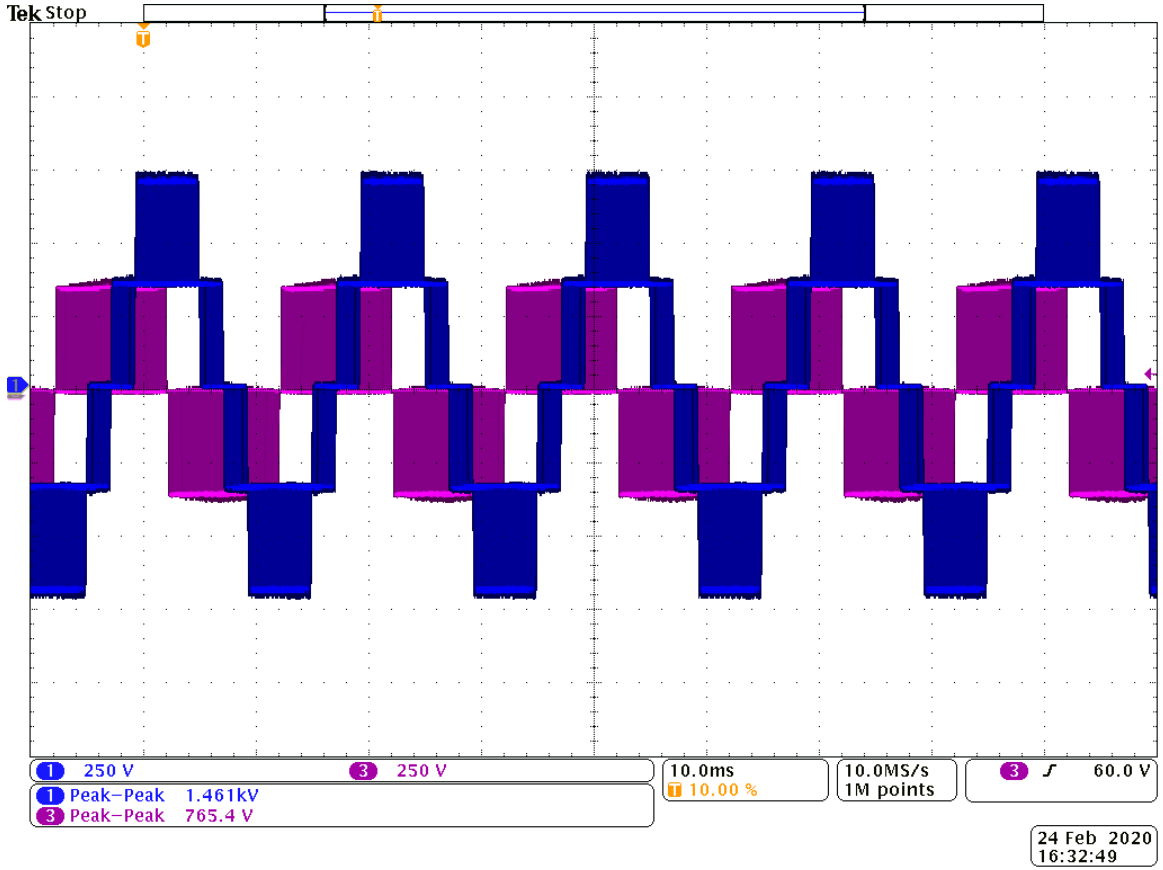
Lab Measurements: 3-Level Modulation

- **Confirms 3-level measurement: V_{CM} = { -350 V, 0 V, +350 V}**





Phase C to Midpoint (V_{CM}) **Phase A to Phase B (V_{AB})**

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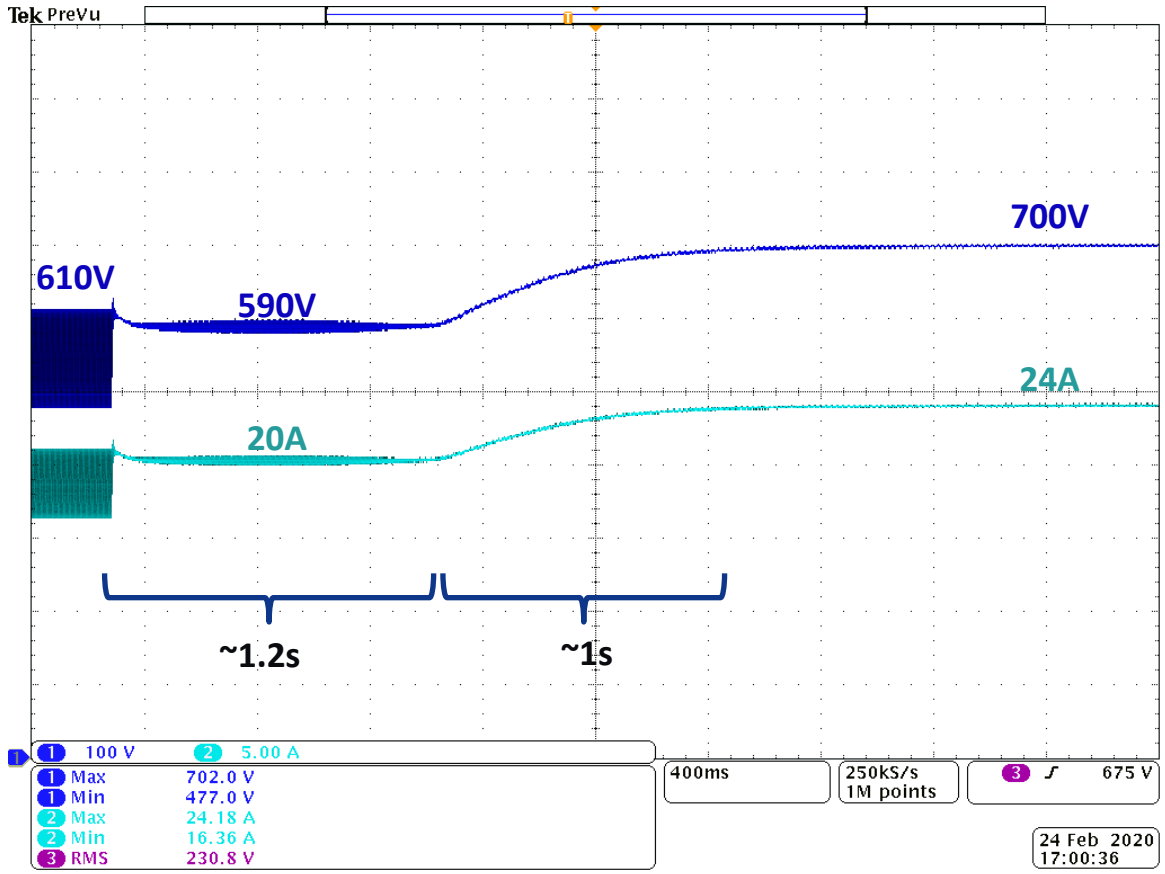
Lab Measurements: PFC Turn-On

- **PFC turn-on into 16 kW load**

DC Output Voltage

DC Output Current



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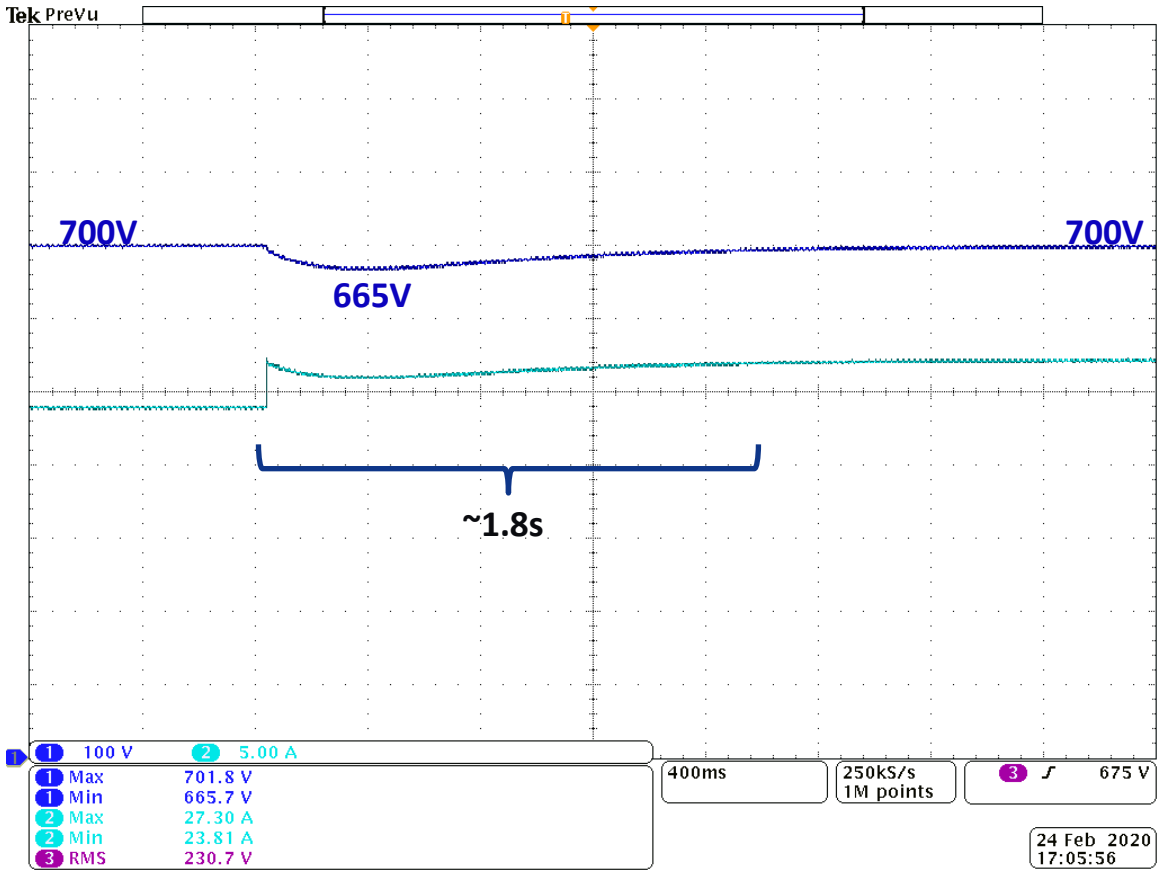
Lab Measurements: Load Step Response

- **Load step from 16 kW to 19 kW**

DC Output Voltage

DC Output Current



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Lab Measurements: Power Meter

- **Efficiency at 27 kW: 98.38 %**
- **Power factor: 0.999**
- **Total harmonic distortion (current): 2.75 8%**
- **MOSFET case temperature: 78 °C**

Normal Mode Uover:- - - - Iover:- - - - U1-3 : 600Vrms Auto YOKOGAWA

& change items Integ:Reset PAGE 1/2

Urms1	398.145 V	Urms3	398.139 V
Irms1	38.9030 A	Irms3	39.0180 A
P1	13.1504 kW	P3	-0.2815 kW
Urms2	398.238 V	Udc4	0.70311 kV
Irms2	39.4527 A	Idc4	37.7202 A
P2	13.8110 kW	P4	26.5215 kW
η1	98.381 %	PΣA	26.9581 kW
F1	99.9091 %	SΣA	26.9826 kVA

Σ A(3V3A): U1A 600Vrms, I1A 50mVrms, U2A 600Vrms, I2A 50mVrms, U3A 600Vrms, I3A 50mVrms

Element4: U4A1000Vdc, I4A 50mVdc

Integ:Reset Time -----:--:--

Efficiency

Power Factor

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Wide-Band Harmonics Uover:- - - - Iover:- - - - PLL Source: U1 YOKOGAWA

PLL	U1
Freq	50.000 Hz
U1	398.119 V
I1	38.9068 A
P1	13.1486kW
S1	15.4839kVA
Q1	-8.1772kvar
λ1	0.84918
ϕ1	328.122 °
Uthd1	0.458 %
Ithd1	2.758 %
Pthd1	0.001 %
Uthf1	0.656 %
Ithf1	2.590 %
Utif1	28.744
Itif1	102.921

Or.	U1 [V]	hdf[%]	I1 [A]	hdf[%]
Tot.	398.119		38.9068	
dc	0.048	0.012	-0.2514	-0.646
1	398.115	99.999	38.8912	99.960
2	0.160	0.040	0.5737	1.475
3	0.036	0.009	0.3827	0.984
4	0.037	0.009	0.1299	0.334
5	0.162	0.041	0.0314	0.081
6	0.084	0.021	0.1930	0.496
7	0.246	0.062	0.1145	0.294
8	0.101	0.025	0.1774	0.456
9	0.089	0.022	0.1187	0.305
10	0.048	0.012	0.0842	0.216
11	0.279	0.070	0.0697	0.179
12	0.121	0.030	0.1025	0.263
13	0.244	0.061	0.0301	0.077
14	0.076	0.019	0.0675	0.173
15	0.044	0.011	0.0307	0.079
16	0.058	0.014	0.0603	0.155
17	0.690	0.173	0.4440	1.141
18	0.046	0.011	0.0146	0.038
19	0.610	0.153	0.3449	0.887
20	0.022	0.006	0.0106	0.027

Σ A(3V3A): U1A 600V, I1A 50mV, U2A 600V, I2A 50mV, U3A 600V, I3A 50mV

Element4: U4A1000V, I4A 50mV

I-THD

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Vienna PFC Reference Design

PLECS Model

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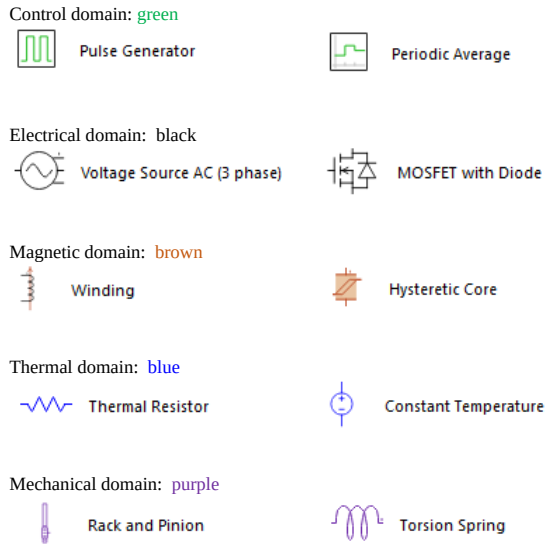
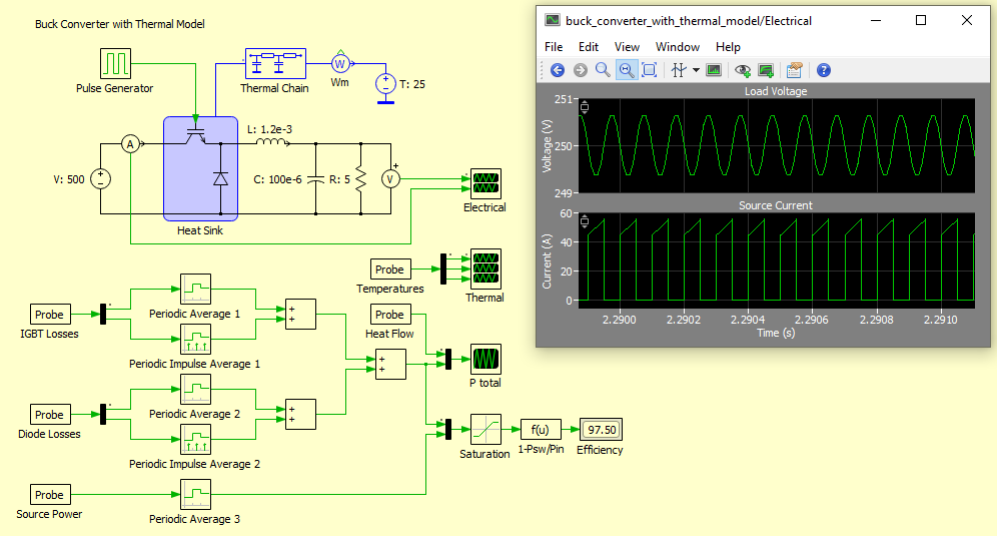
PLECS Software

- Piecewise-Linear Electrical Circuit Simulation (PLECS) by Plexim
- Power electronics circuits and systems simulation tool
- PLECS Standalone vs PLECS Blockset
  - Blockset operates in Simulink environment
  - Standalone equipped with its own processing engine and runs faster
  - Models can be exchanged between the two versions
  - Microchip-purchased license: Single license of PLECS Standalone
- Uses ideal switches to quickly and efficiently simulate dynamic behavior of complex systems
- Multi-domain approach to simultaneously simulate the control, electrical, magnetic, thermal, and mechanical domains
- Supports Processor-In-the-Loop (PIL) and Hardware-In-the-Loop (HIL)
- Similar tools: Matlab/Simulink, PSIM, Opal RT, SaberRD
- SiC competitors providing reference designs and component models in PLECS

- Demo mode available, allows users to build and simulate models (cannot save model, session limited to 60 minutes, and no PIL)

- Plexim currently offering 90-day trial license (Video walk-through of PLECS Standalone installation)
  - Windows: https://www.plexim.com/support/videos/installing-standalone-win
  - Mac: https://www.plexim.com/support/videos/installing-standalone-mac
  - When requesting license, select PLECS Standalone and PIL





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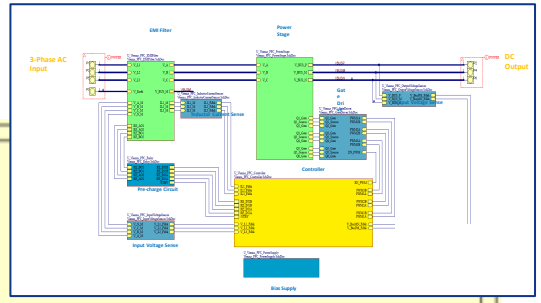
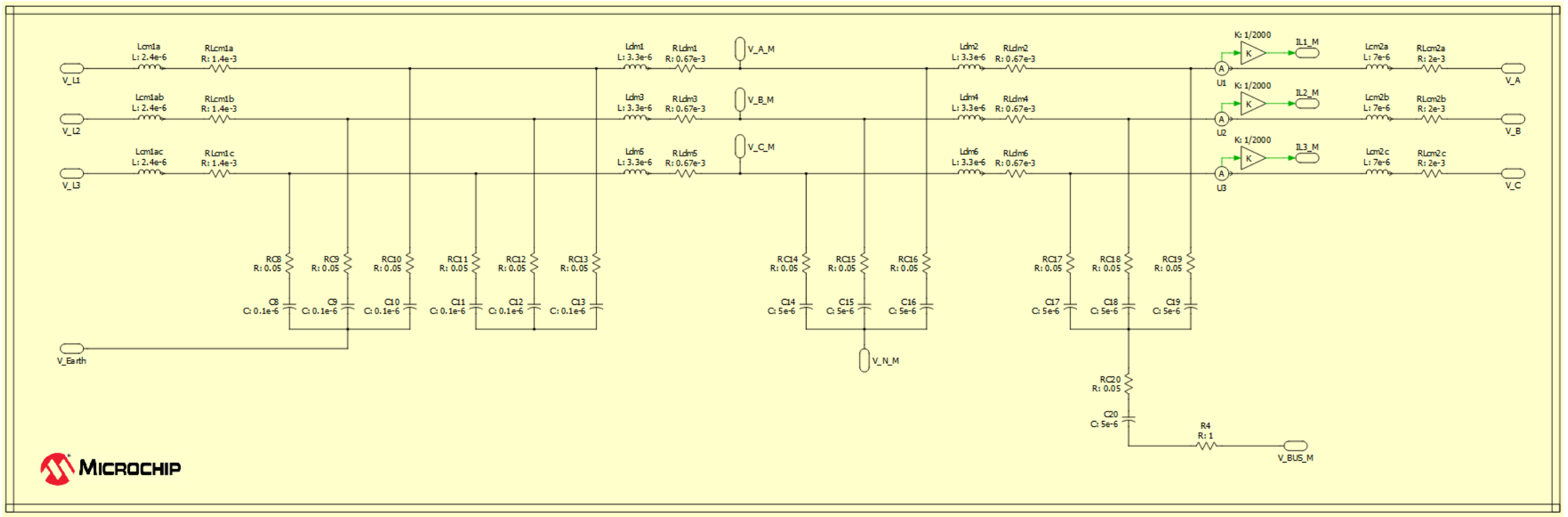
Top-Level Model

Reference Design Schematic



EMI Filter

- Differential filters, common-mode filtering not implemented
- Mid-point feedback path
- AC voltage measurement points
- AC current sensor



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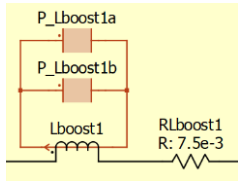
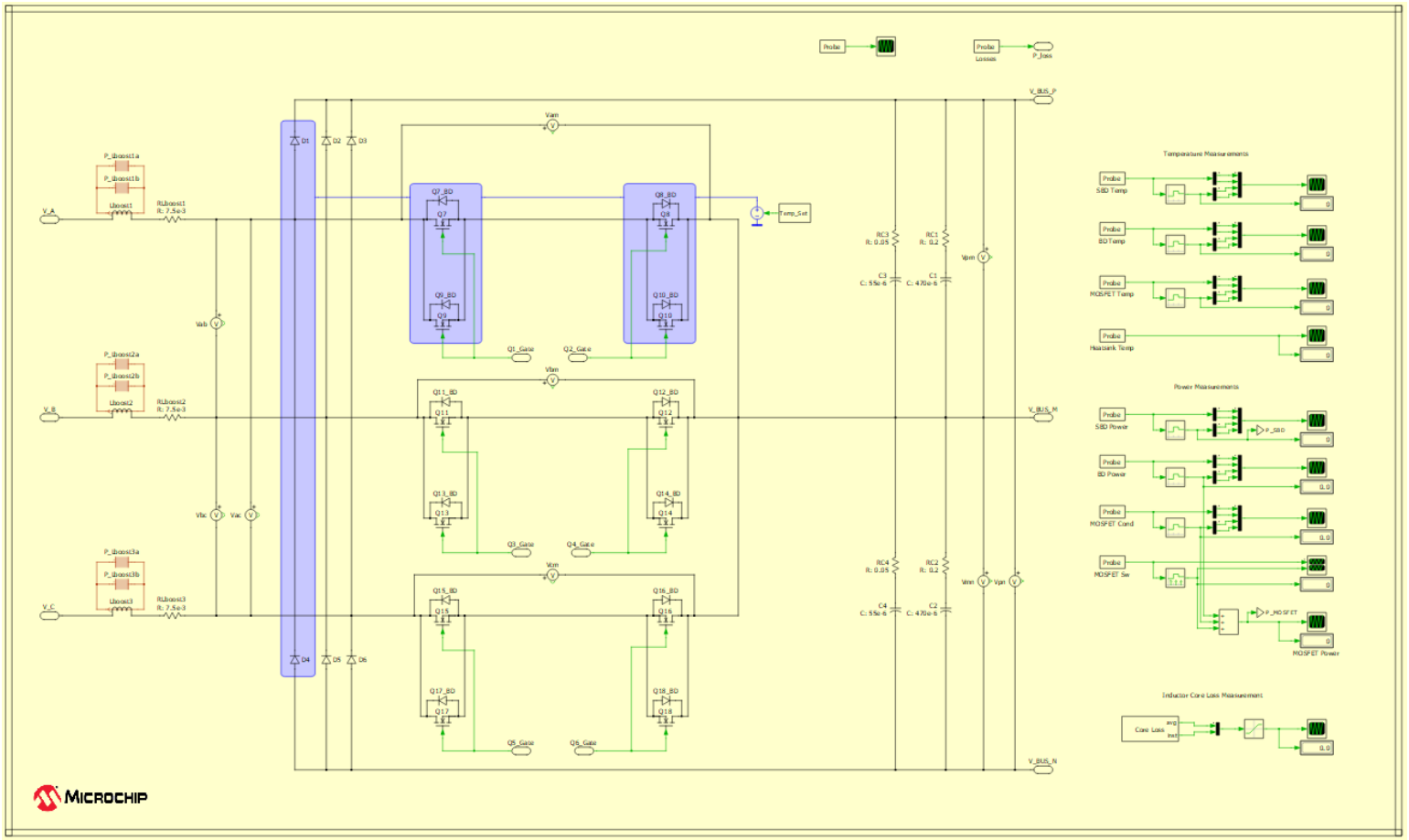
Power Stage

- **Power Stage Model**
  - With PLECS thermal domain
  - Without PLECS thermal domain (faster simulation)
- **Thermal Model**
  - Heat sink thermal resistance and thermal capacitance
  - Thermal capacitance reduced for faster simulation
  - Characteristics defined in mask
  - SiC Schottky barrier diode model (MSC050SDA120B)
  - SiC MOSFET model (MSC015SMA070B)
  - Loss and temperature available on scopes
- **Boost inductor model**
  - PLECS magnetic domain
  - 20-turn winding
  - Two cores
  - Characteristics defined in mask
  - Core loss based on magnetic flux density vs core loss curve from datasheet
  - Copper loss modeled by DCR





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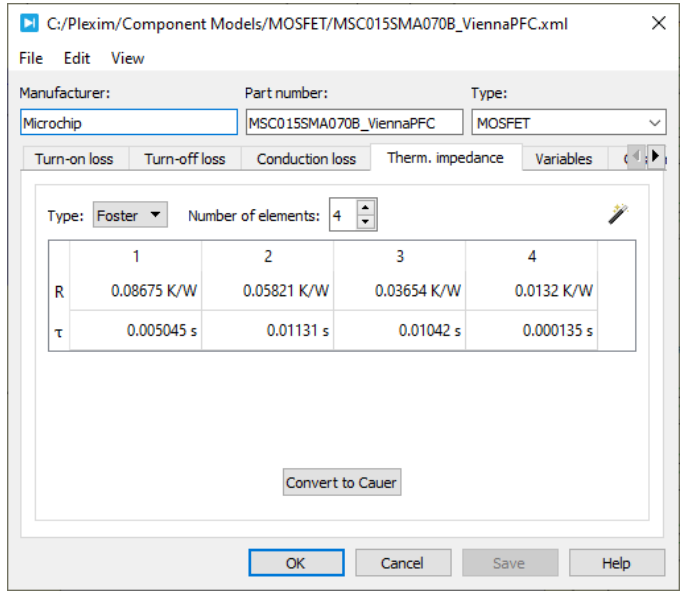
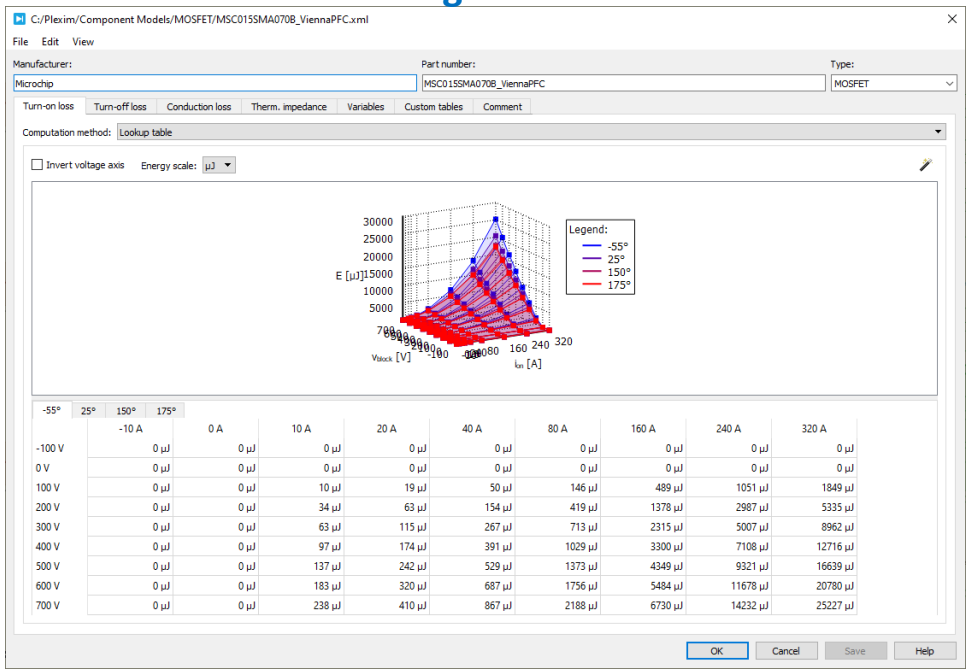
Component Model

- PLECS component model is named a Thermal Description
- Lookup tables for conduction loss, turn-on loss, and turn-off loss based on V, I, T
- Supports additional dependencies such as R_G or dV/dt
- Thermal impedance (Foster or Cauer network)
- MOSFET body diode modeled as separate diode
- PLECS models for all SiC discrete devices planned for this quarter

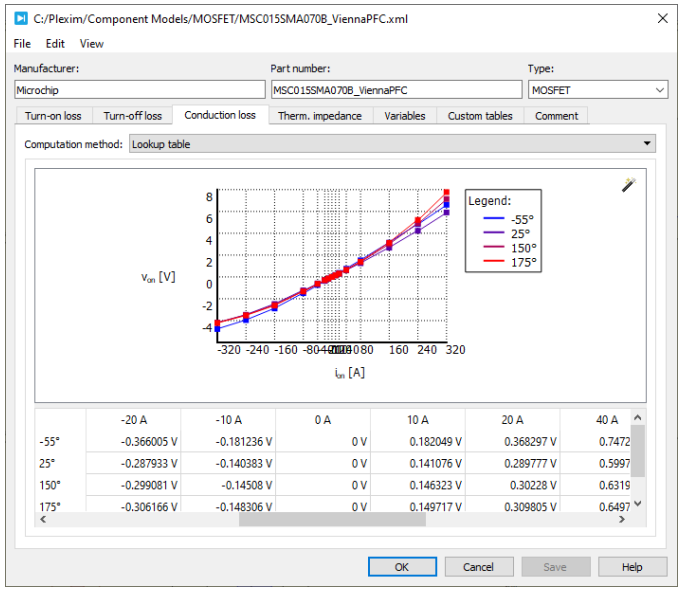
Thermal Network



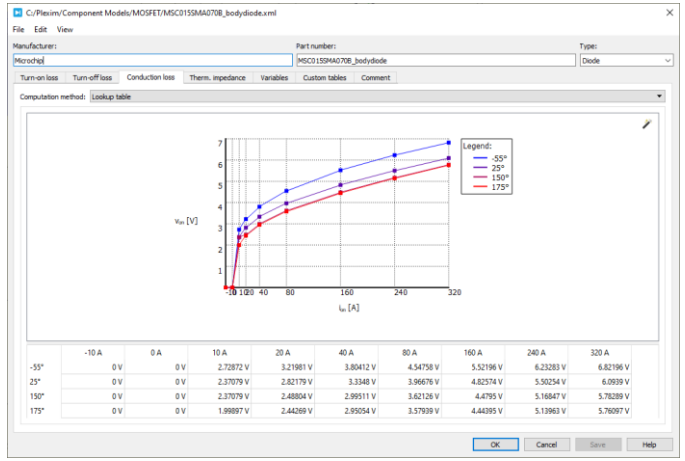
Switching Losses



Conduction Loss



Body Diode Conduction Loss



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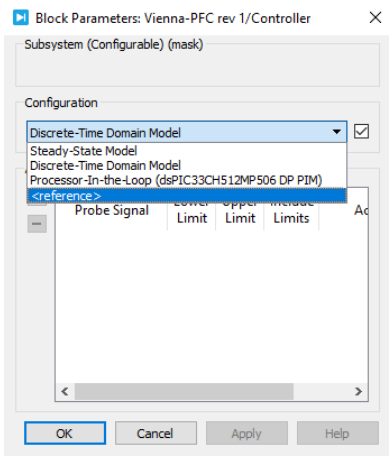
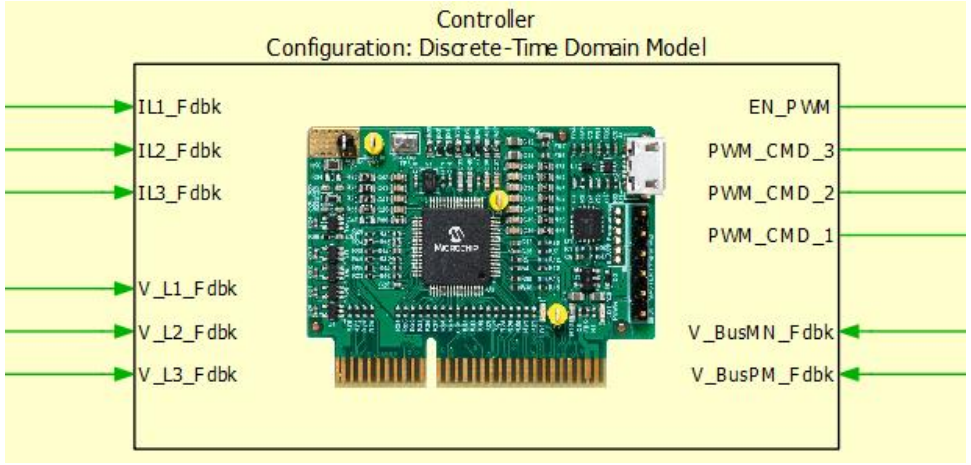
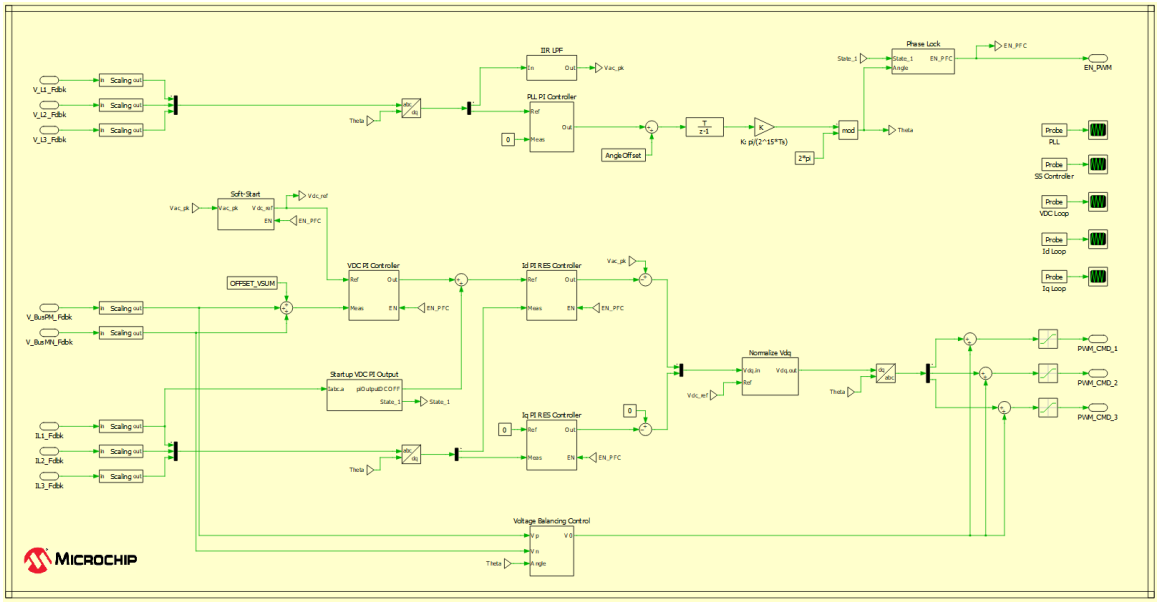
Controller

- **Controller Models**
  - Steady-State Model
  - Discrete-Time Domain Model
  - Processor-In-the-Loop (PIL)

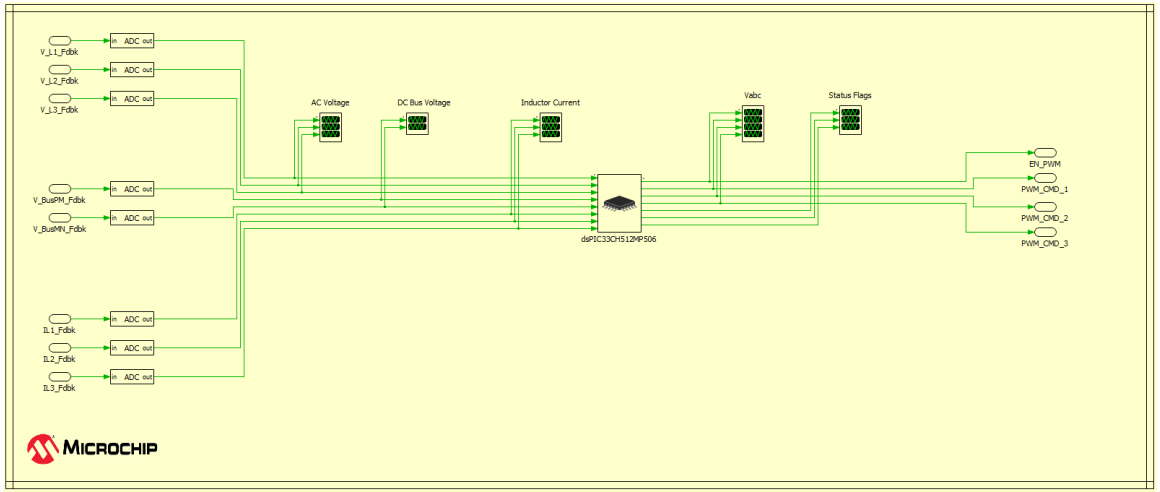




Control Algorithm Model



Control Algorithm Running on dsPIC33 DSC



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Voltage & Current Sensing

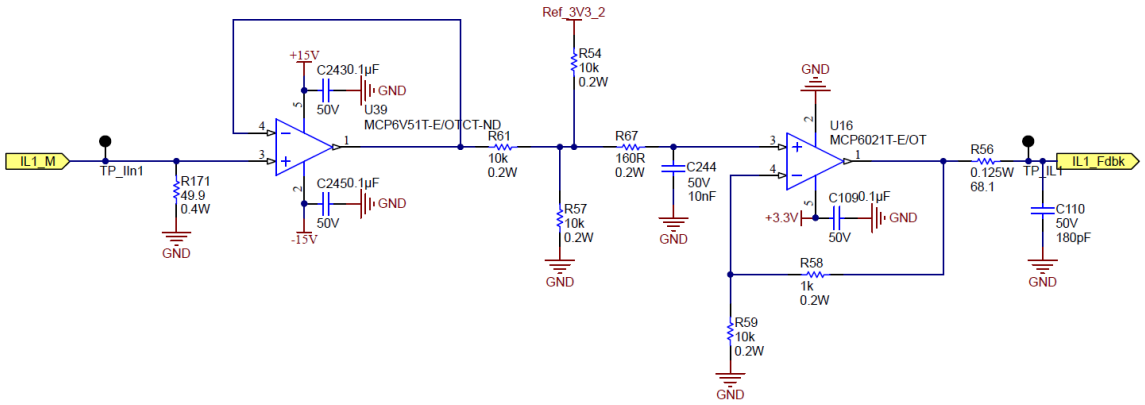
- **Sense circuits modeled in control domain**
  - Gain
  - Offset
  - Transfer function
- **Faster simulation than electrical domain**
- **Component values defined as local variables in the mask**
- **Includes RC filter on PIM (R63 & C33)**

Mask

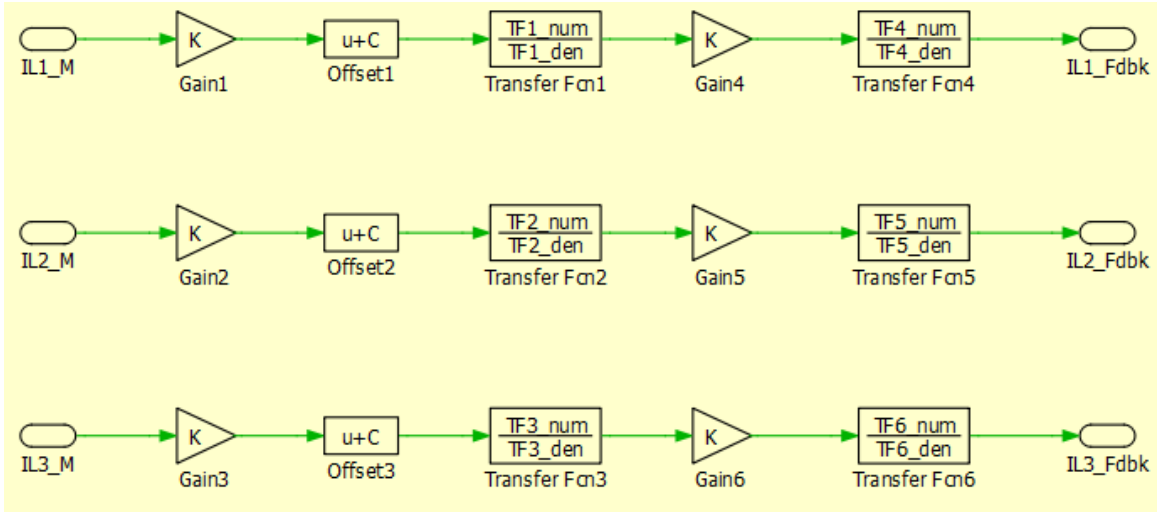
```
Ref_3V3_2=3.3;

% IL1 Current Sense
R171=49.9;
R61=10e3;
R54=10e3;
R57=10e3;
C244=10e-9;
R67=160;
R58=1e3;
R59=10e3;
R56=68.1;
C110=180e-12;
R63=150;
C33=560e-12;
Gain1=R171*((R57*R54)/(R57+R54))/(R61+((R57*R54)/(R57+R54)));
Offset1=Ref_3V3_2*((R57*R54)/(R57+R54))/(R61+((R57*R54)/(R57+R54)));
TF1_num=[1];
TF1_den=[((R61^-1+R54^-1+R57^-1)^-1+R67)*C244 1];
Gain4=1+R58/R59;
TF4_num=[1];
TF4_den=[(R56*R63*C110*C33) (R56*C110+R56*C33+R63*C33) 1];
...
```

Inductor Current Sense Circuit



Inductor Current Sense Model



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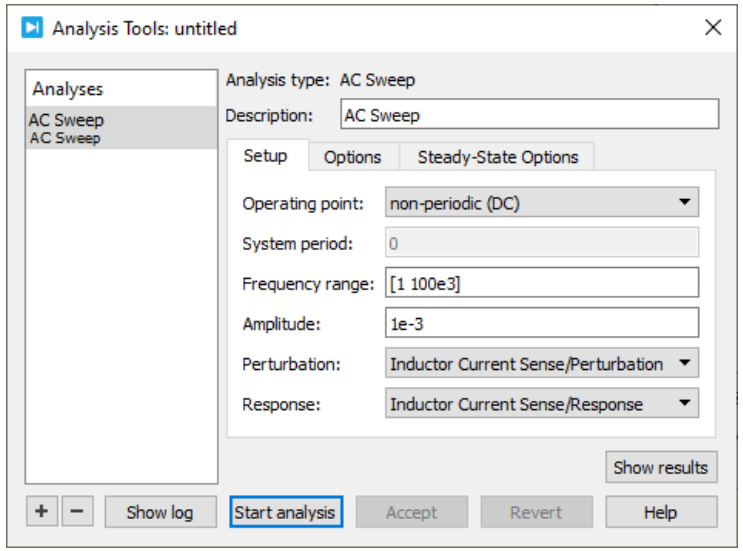
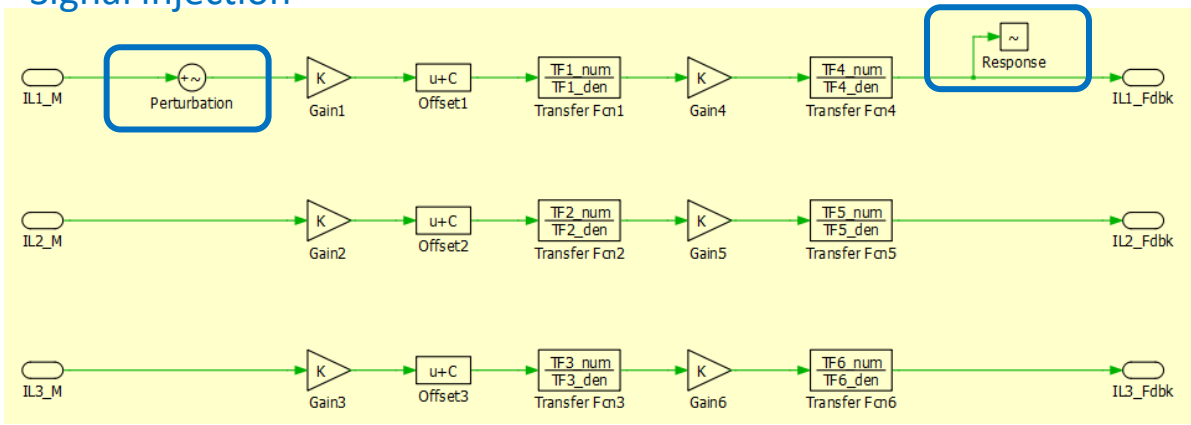
Bode Plot

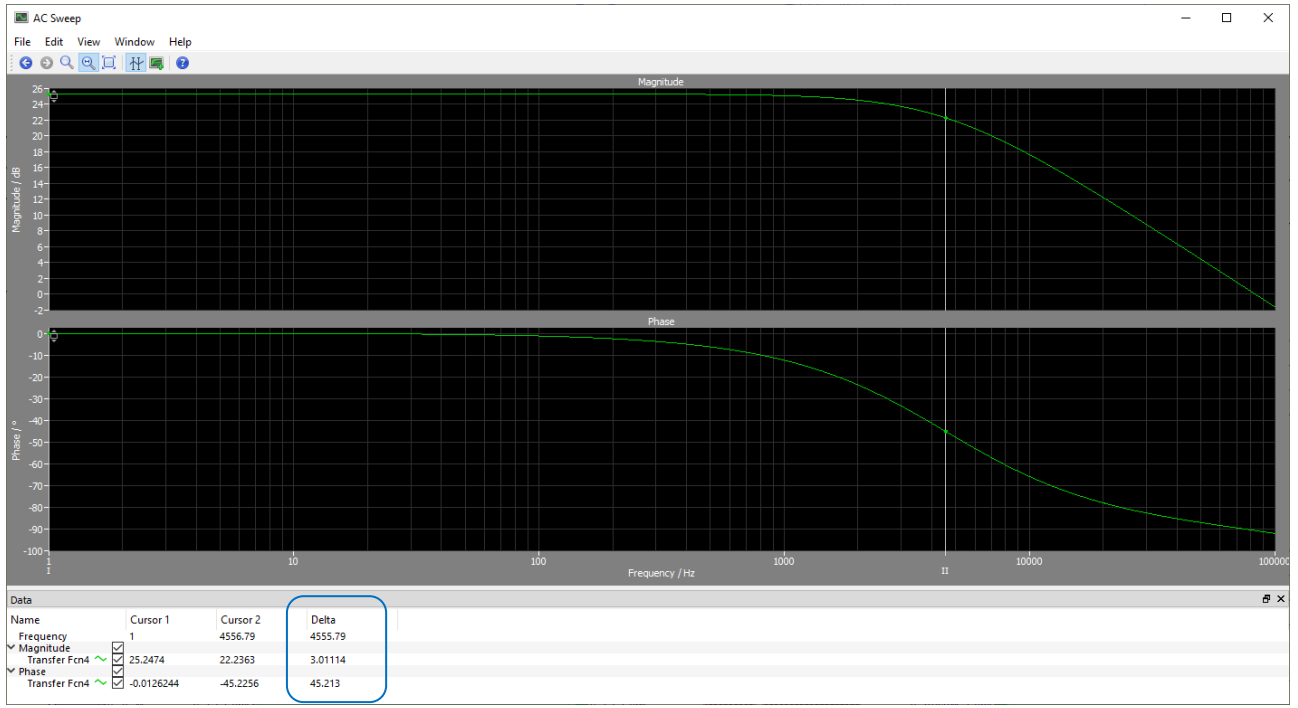
- **PLECS analysis tools**
  - Steady-state analysis
  - AC sweep
  - Impulse response
  - Multitone analysis
- **AC sweep of Current Sense Model**
  - Add perturbation signal and response components
  - Setup analysis as below



Signal injection

Measurement





fc = 4.5kHz

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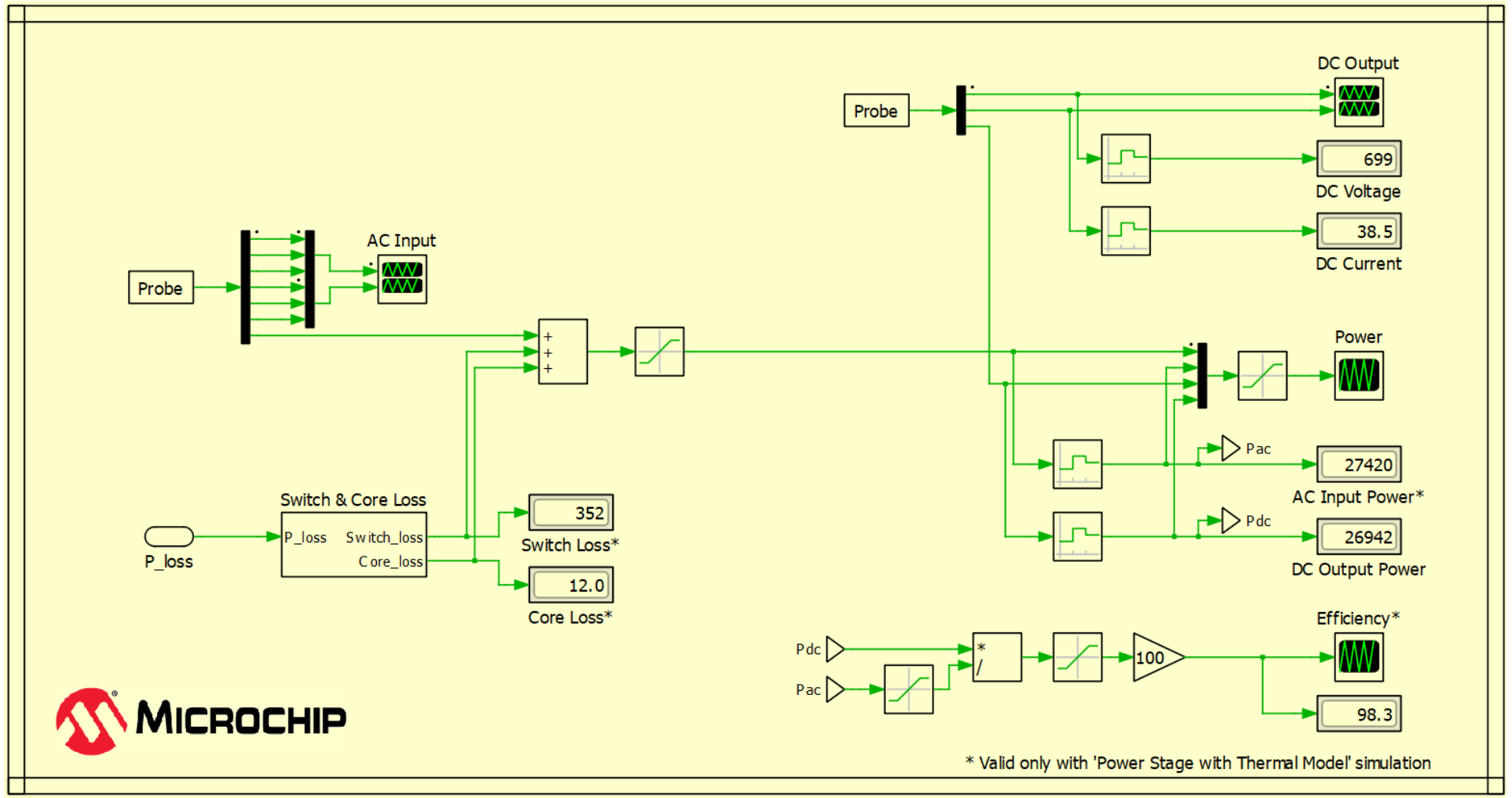
Power Meter

- To ease analysis of the model, a power meter is included to display currents, voltage, power, and efficiency



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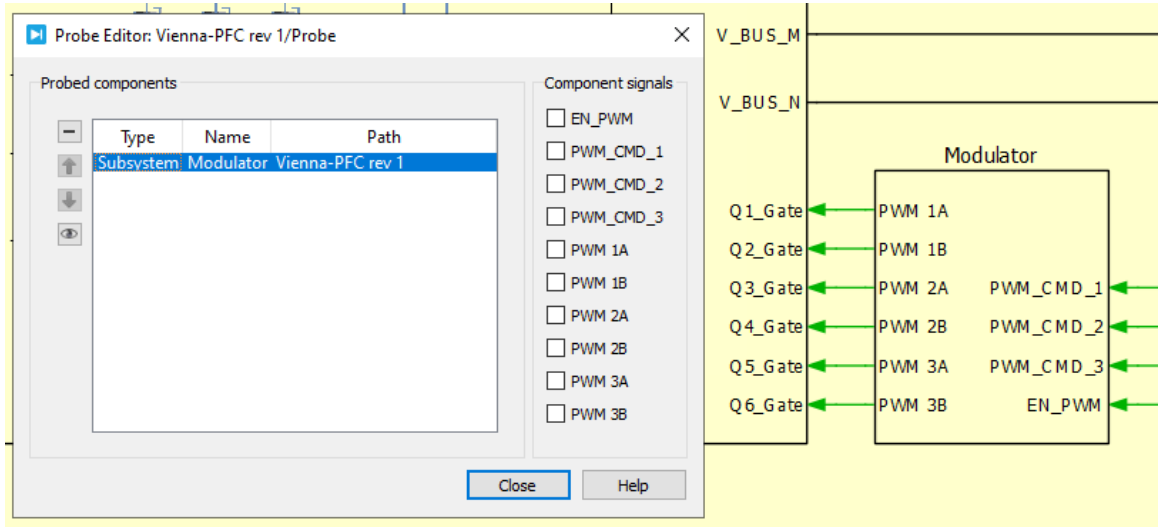
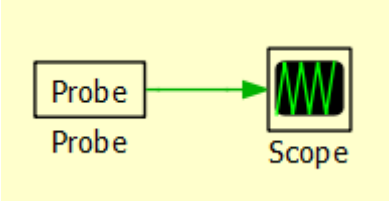
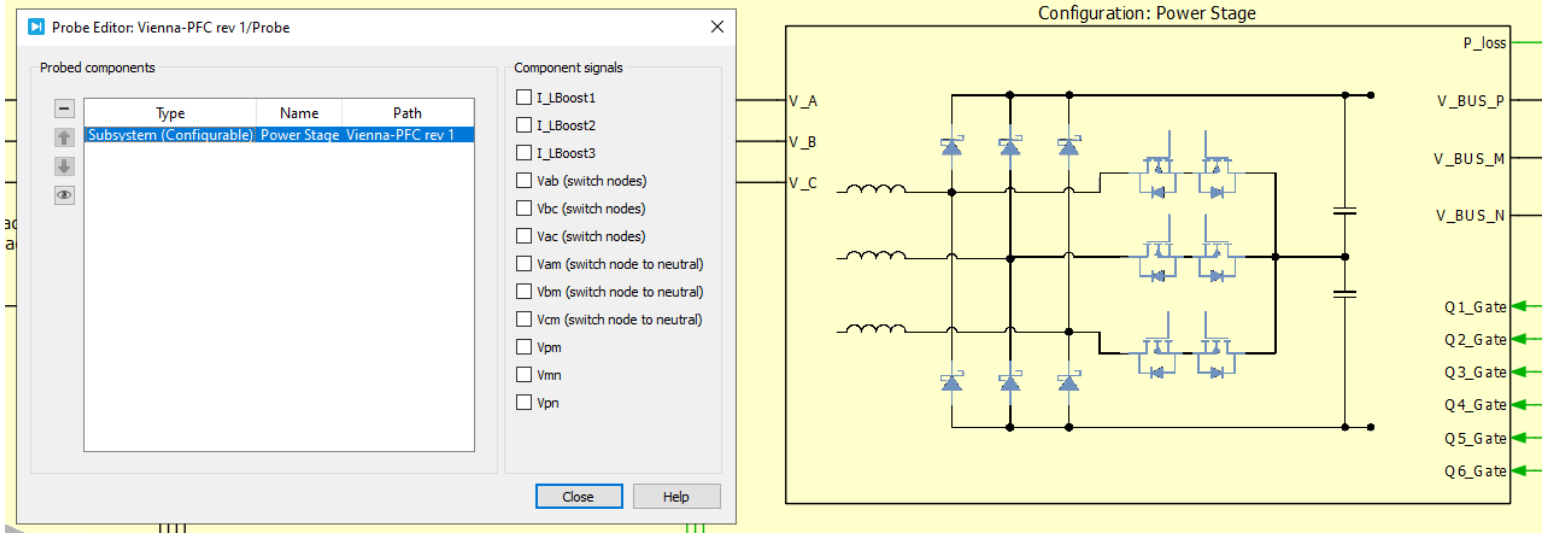
Signal Monitoring

- **Many subsystems setup with ‘probe’ signals for easy monitoring**

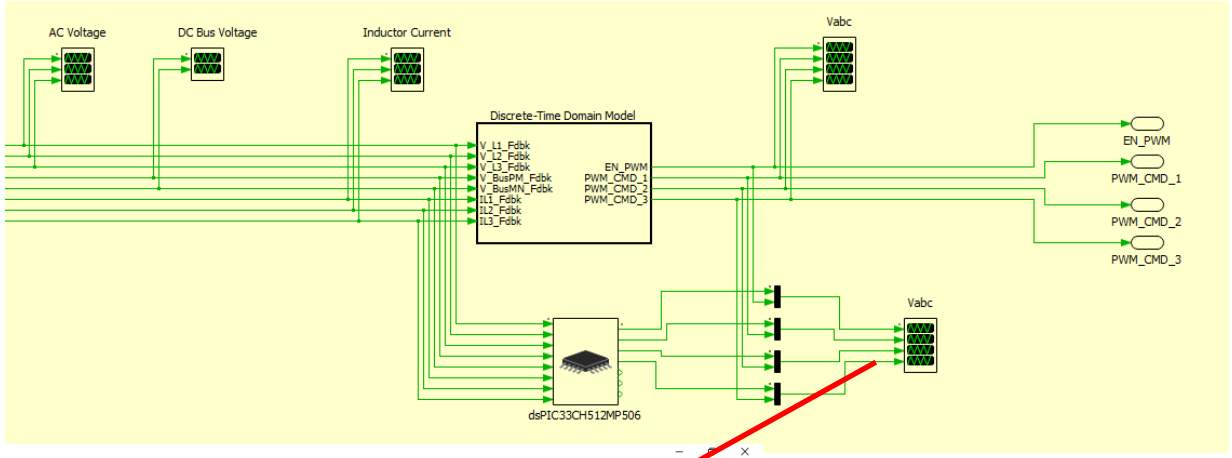


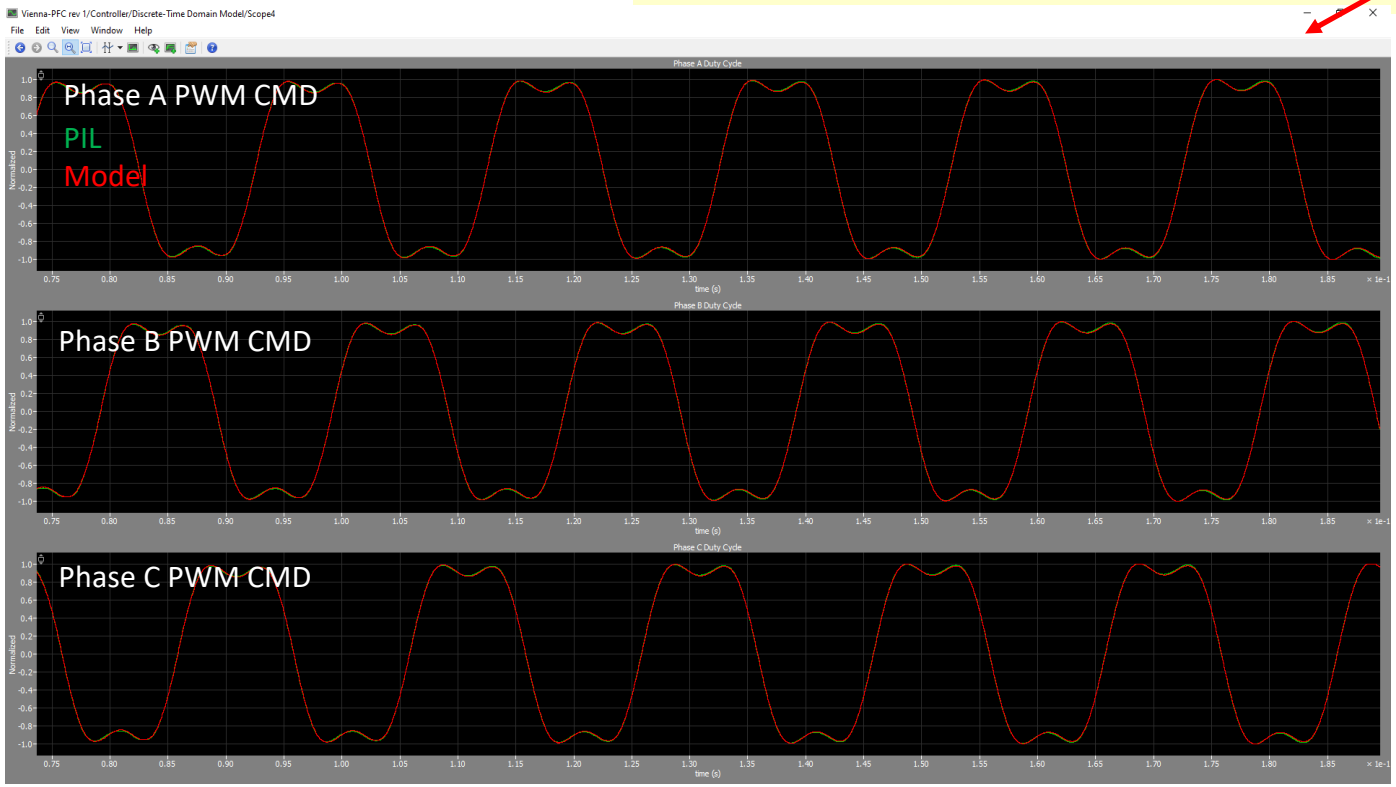




Simulation Results: Model vs PIL

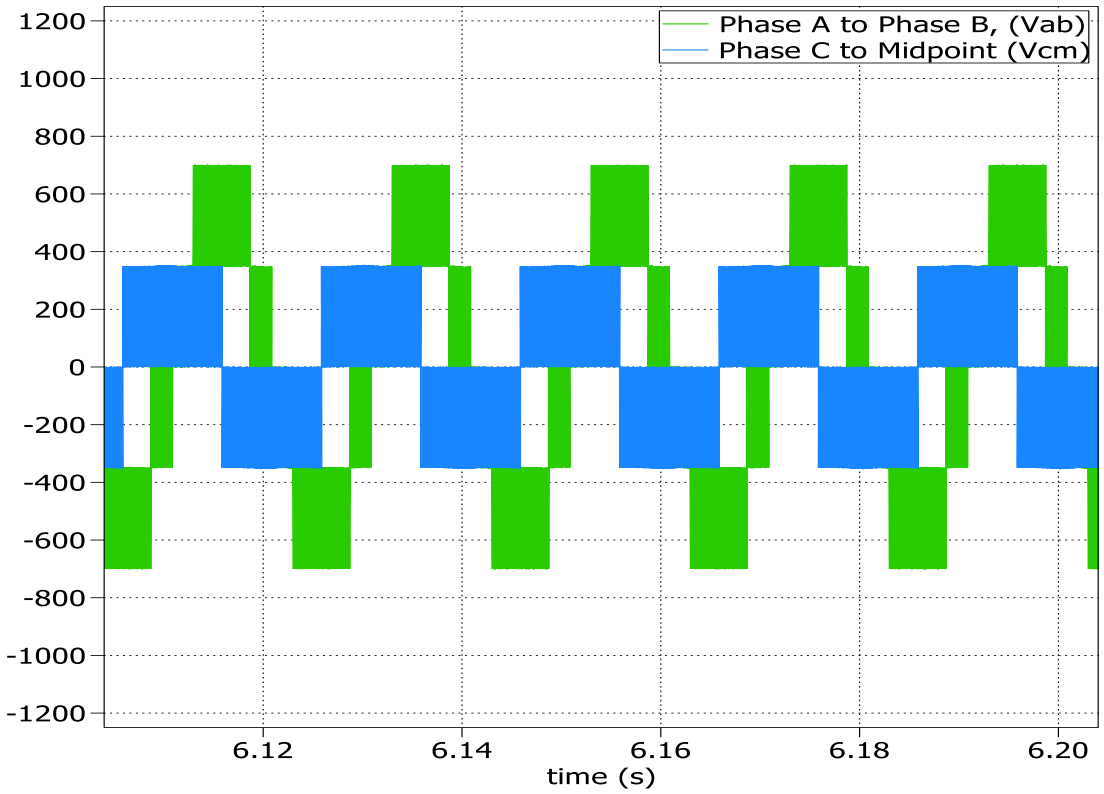
- To verify accuracy of model, connected processor open-loop in order to compare PWM outputs
- Result below shows model and processor produced nearly identical PWM values



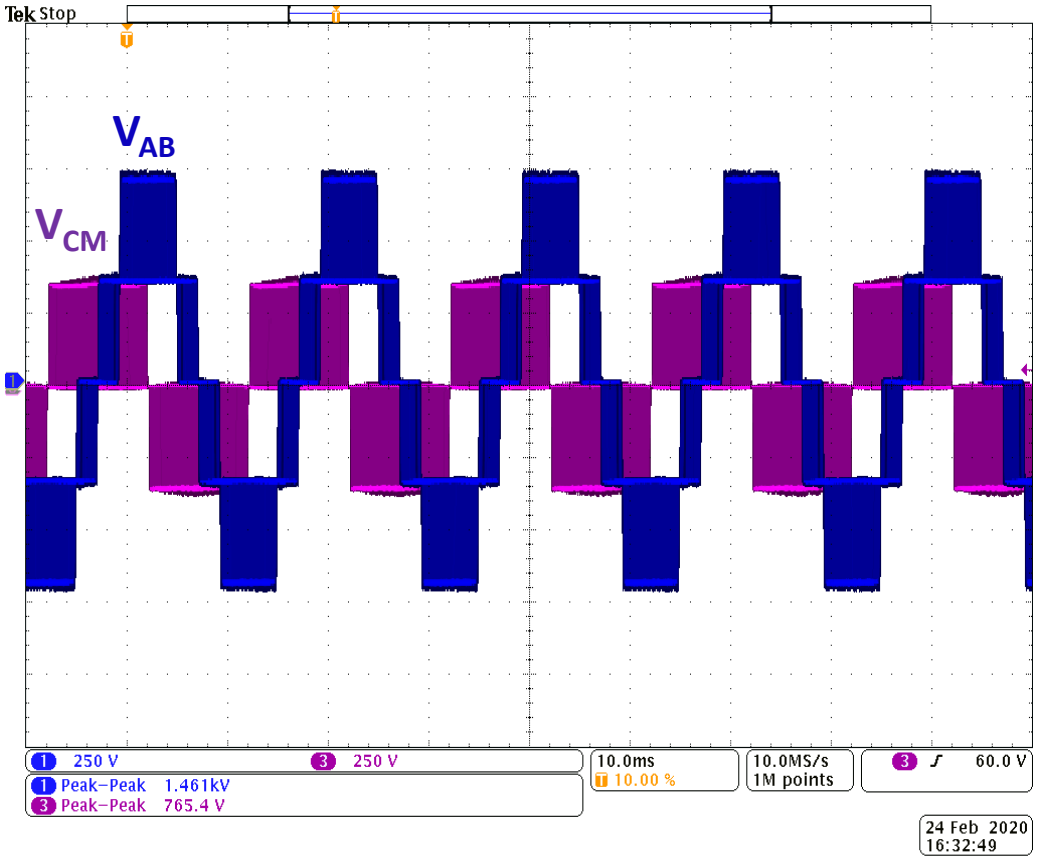


Simulation Results: 3-Level Modulation

Simulation Results



Lab Measurement



V_{CM} = { -351V, 0V, 352V }

V_{AB} = { -700V, -350V, 0V, 351V, 700V }

Simulation result matches expected behavior

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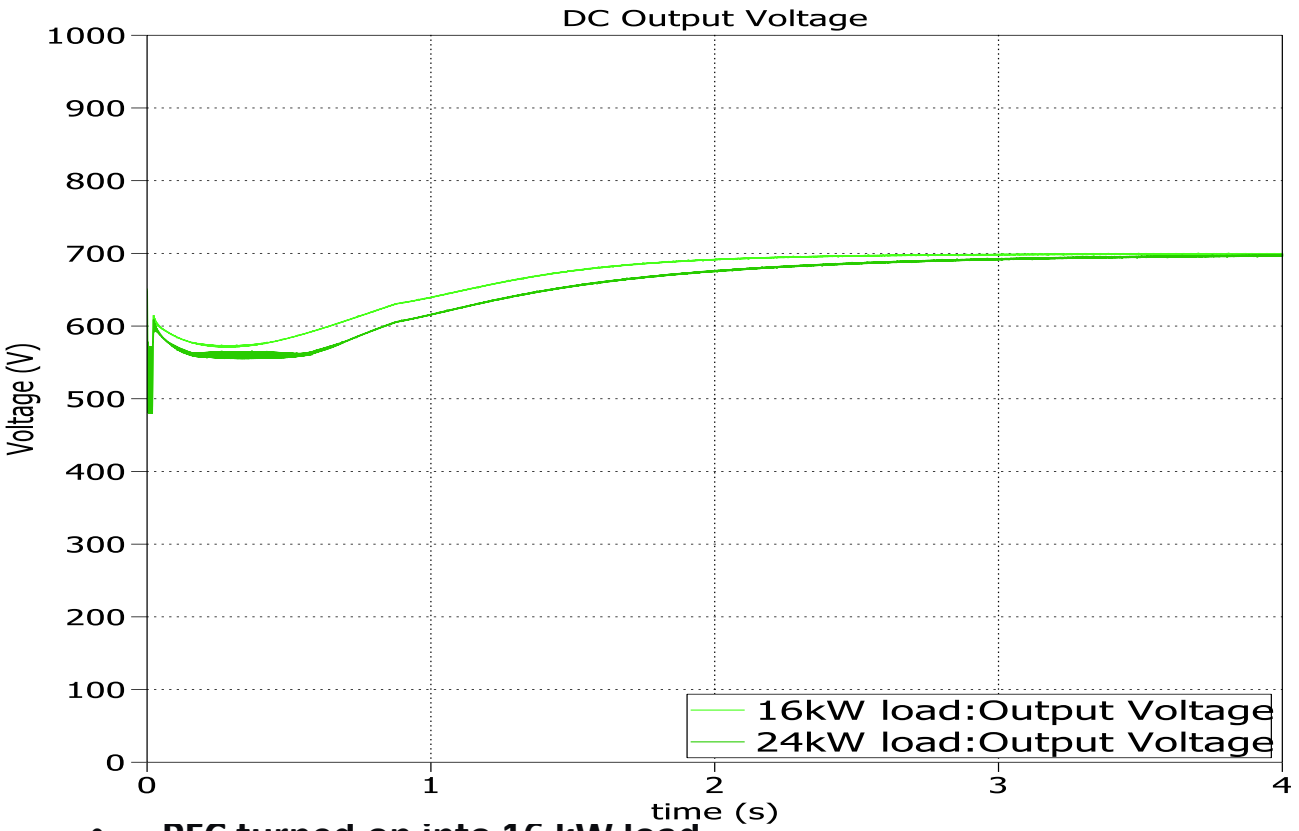
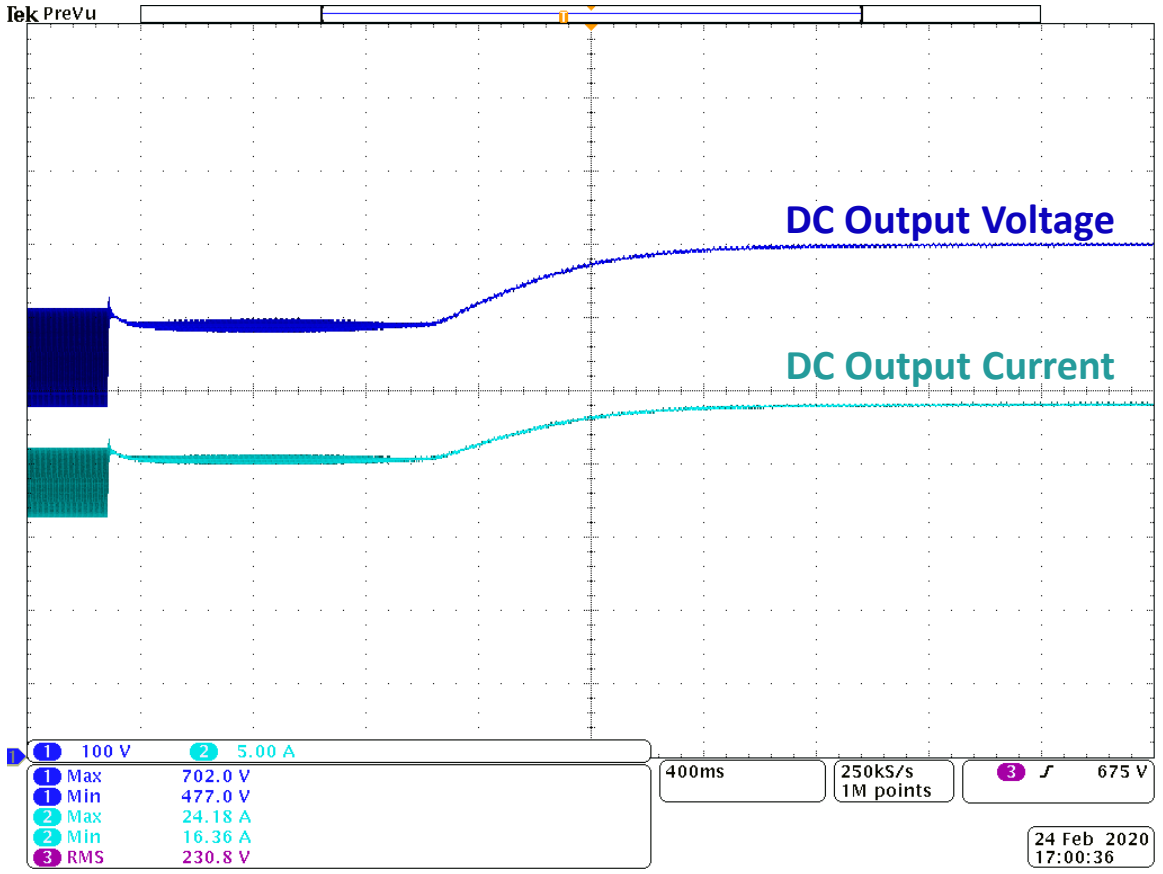
Simulation Results: PFC Turn-On

Simulation Results



Lab Measurement (16kW load)



- PFC turned on into 16 kW load
- Some differences in waveform signature and duration of lab measurement vs simulation at 16 kW
- May be differences in test conditions or unaccounted propagation delays

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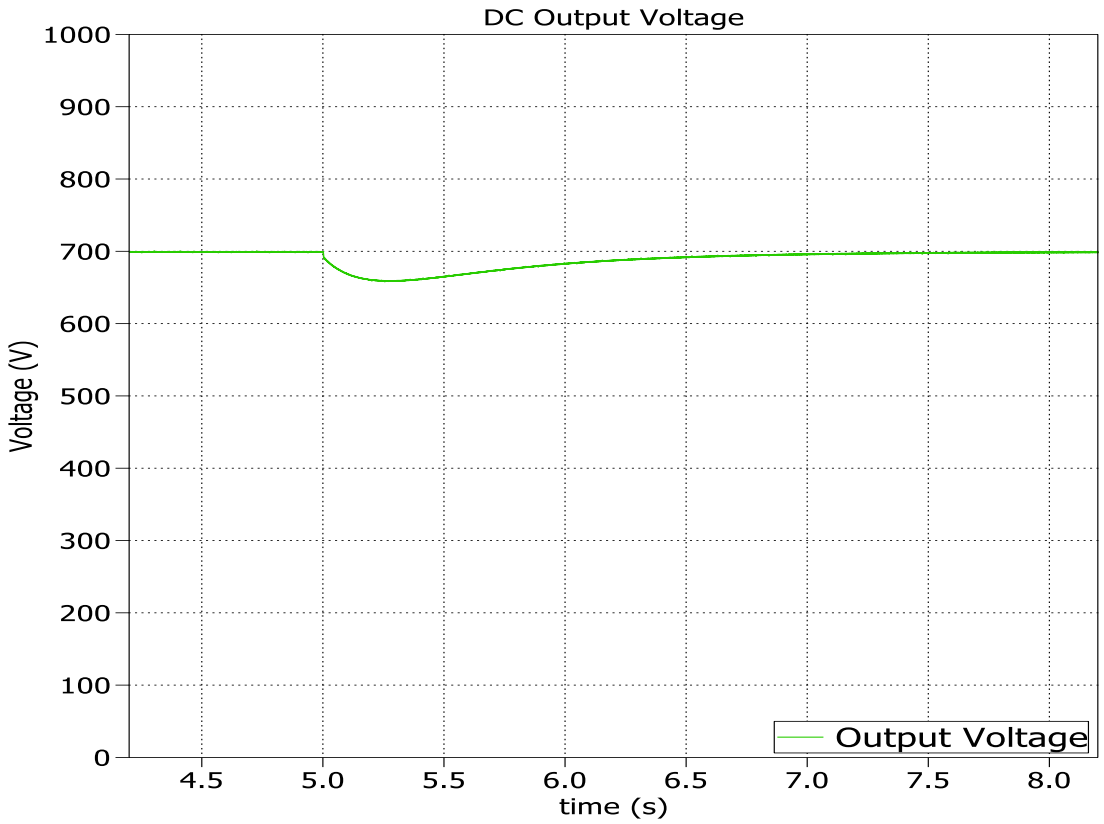
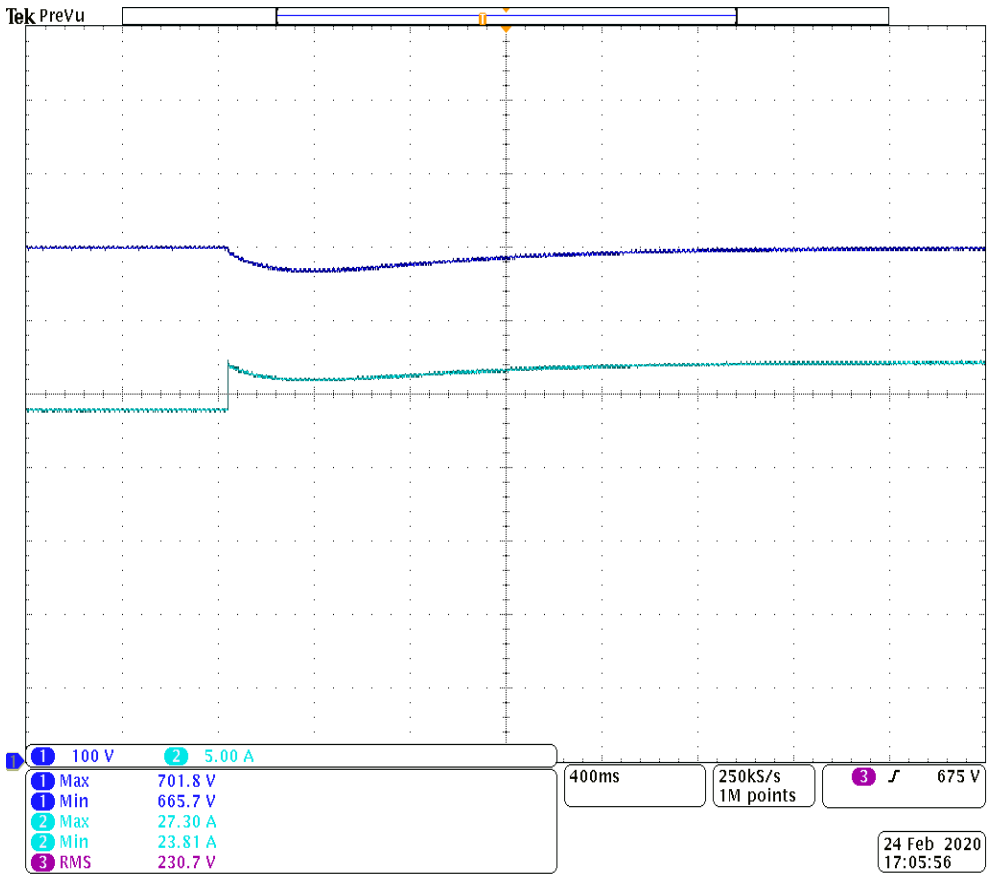
Simulation Results: Load Step Response

Simulation Results



Lab Measurement



- Load step from 16 kW to 19 kW
- Waveform signature, amplitude, and duration of lab measurement and simulation correlate well
- Confirms controller and plant models match physical hardware

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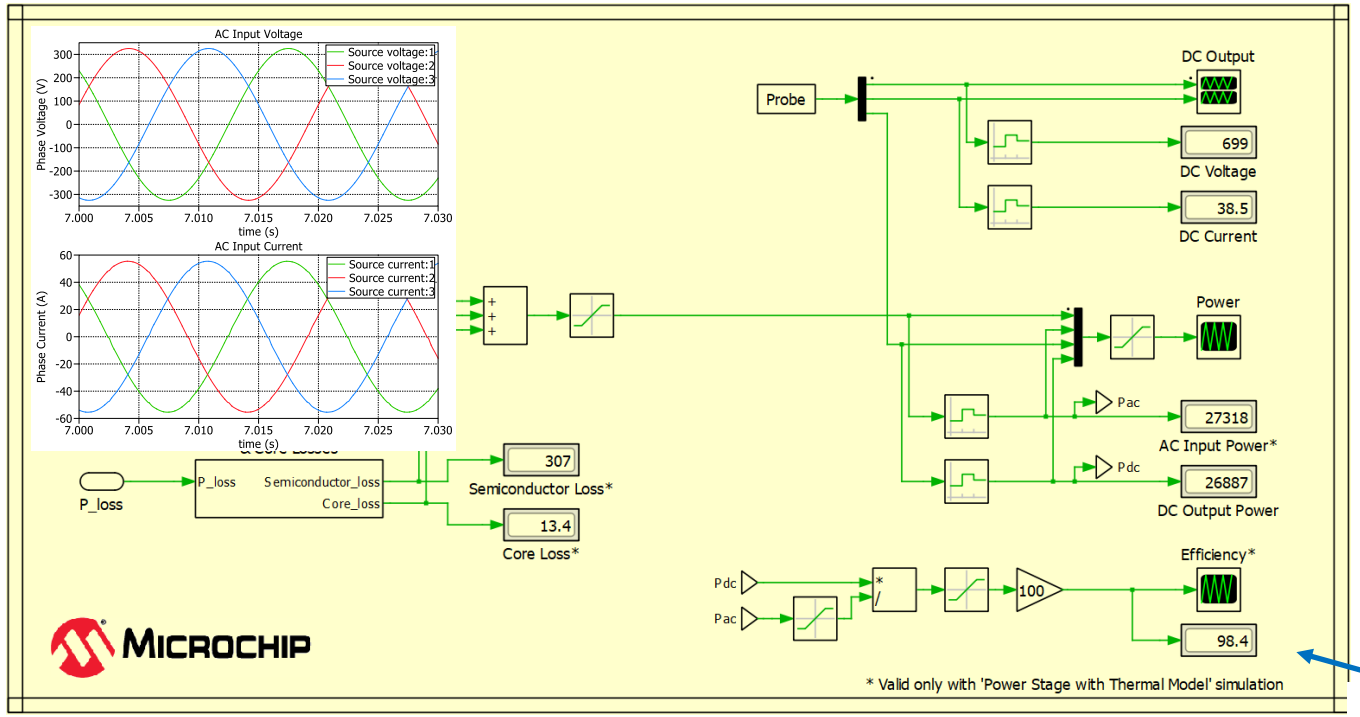
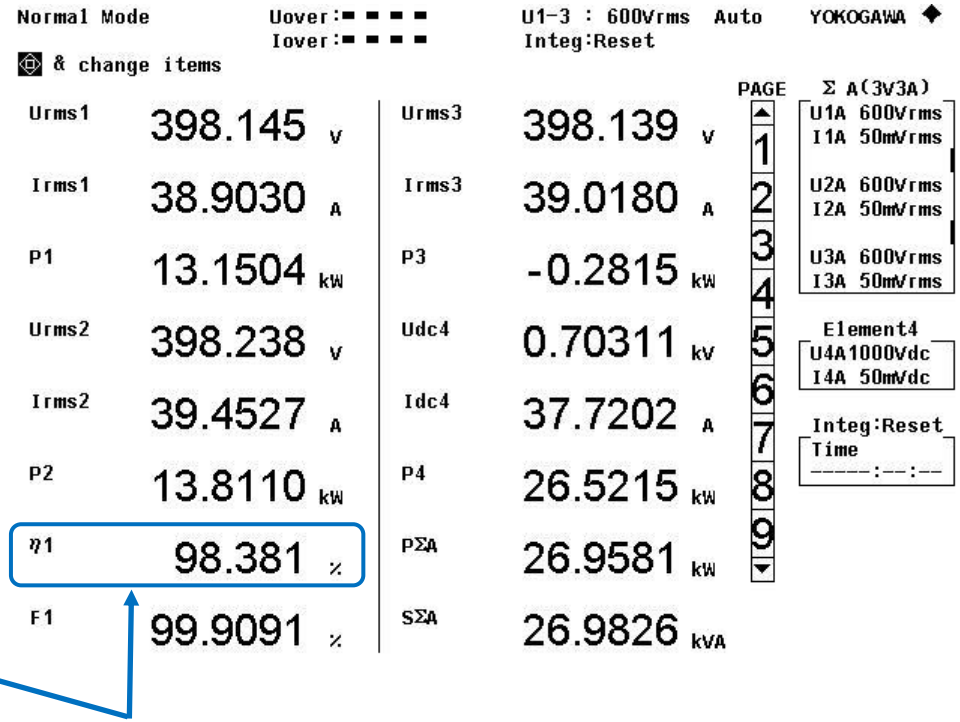
Simulation Results: Efficiency

Simulation Results



Lab Measurement



Efficiency

- Simulated with 27 kW output power to match lab measurement conditions
- Efficiency in lab measurement is 98.38 %, simulation is 98.43 %

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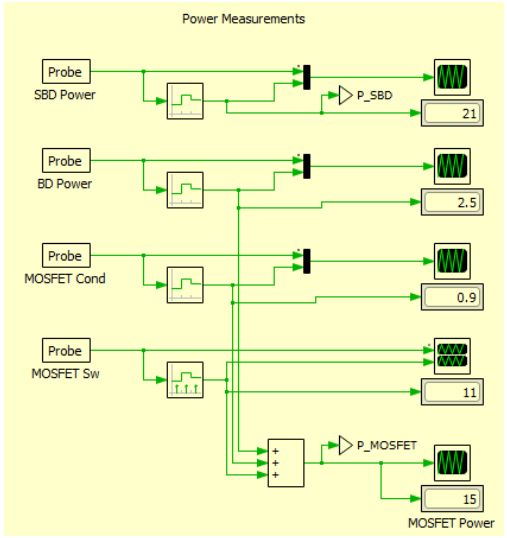
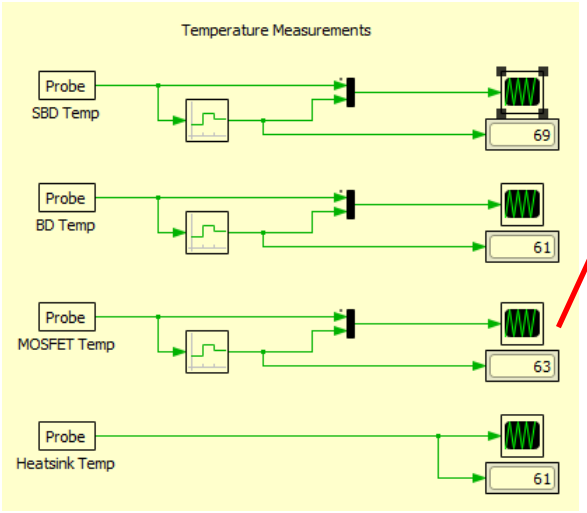
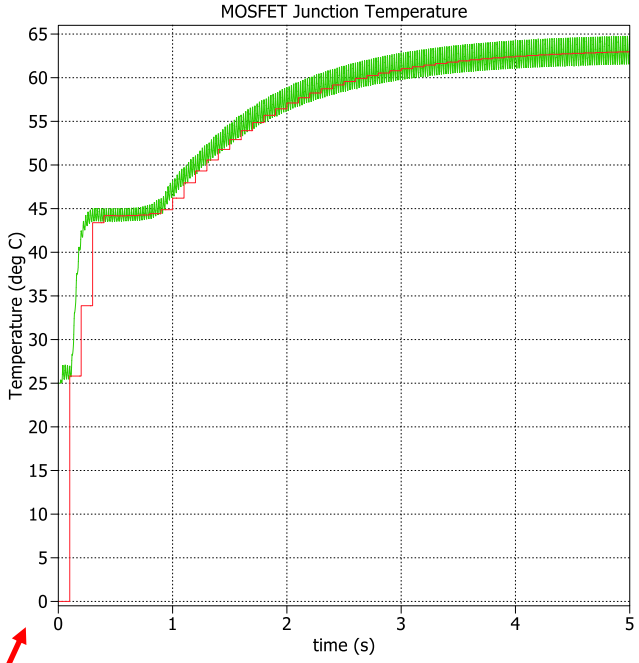
Simulation Results: Thermal

Simulation Results







Lab Measurement

- Simulated with 27 kW output power to match lab measurement conditions
- MOSFET temperature in lab measurement is 78 °C, simulation is 63 °C
- Difference may be related:
  - Non-uniform heat distribution on heat sink, resulting in higher thermal resistance
  - Increased heat sink thermal resistance due to boost inductor restricting air flow
  - Component tolerances
- MOSFET temperature ripple: $15W * 0.2\frac{°C}{W} = 3°C$

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Key Takeaways

- 30 kW Vienna PFC Reference Design available at www.microchip.com/PFC
- Reference Design package includes design files, software, and user's guide (no hardware)
- PLECS is a multi-domain, behavioral simulation environment and powerful tool enabling users to evaluate, modify, analyze, tune, and debug the Vienna PFC Reference Design
- Plexim currently offering 90-day trial license https://www.plexim.com/support/videos/installing-standalone-win
- Demo mode available, session limited to 60 minutes

Thank You

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