Introduction to Digital Controlled Totem-pole PFC Demo Board: Hardware Design

Transphorm Inc.

12/01/2021

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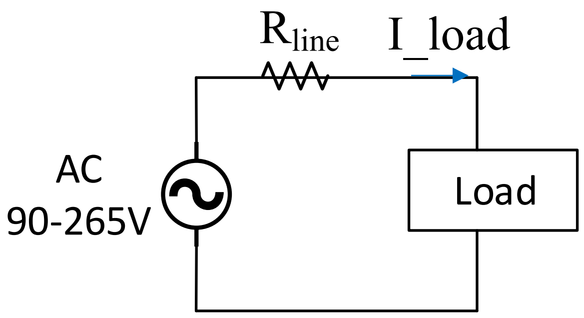
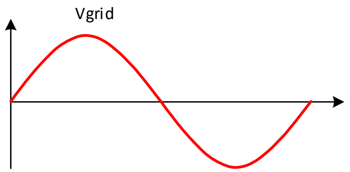
Highest Performance, Highest Reliability GaN

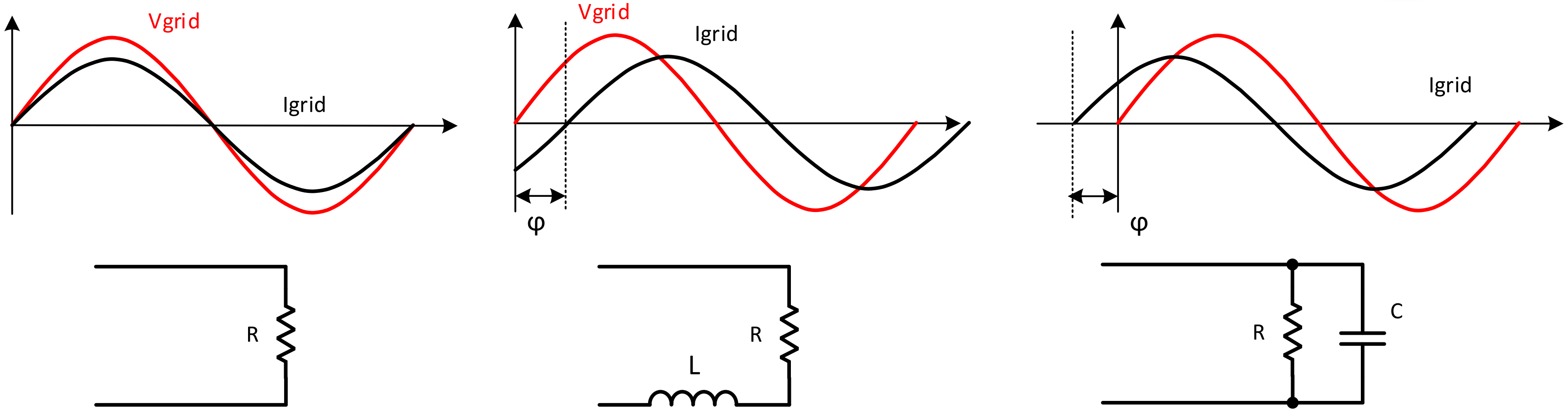
Agenda

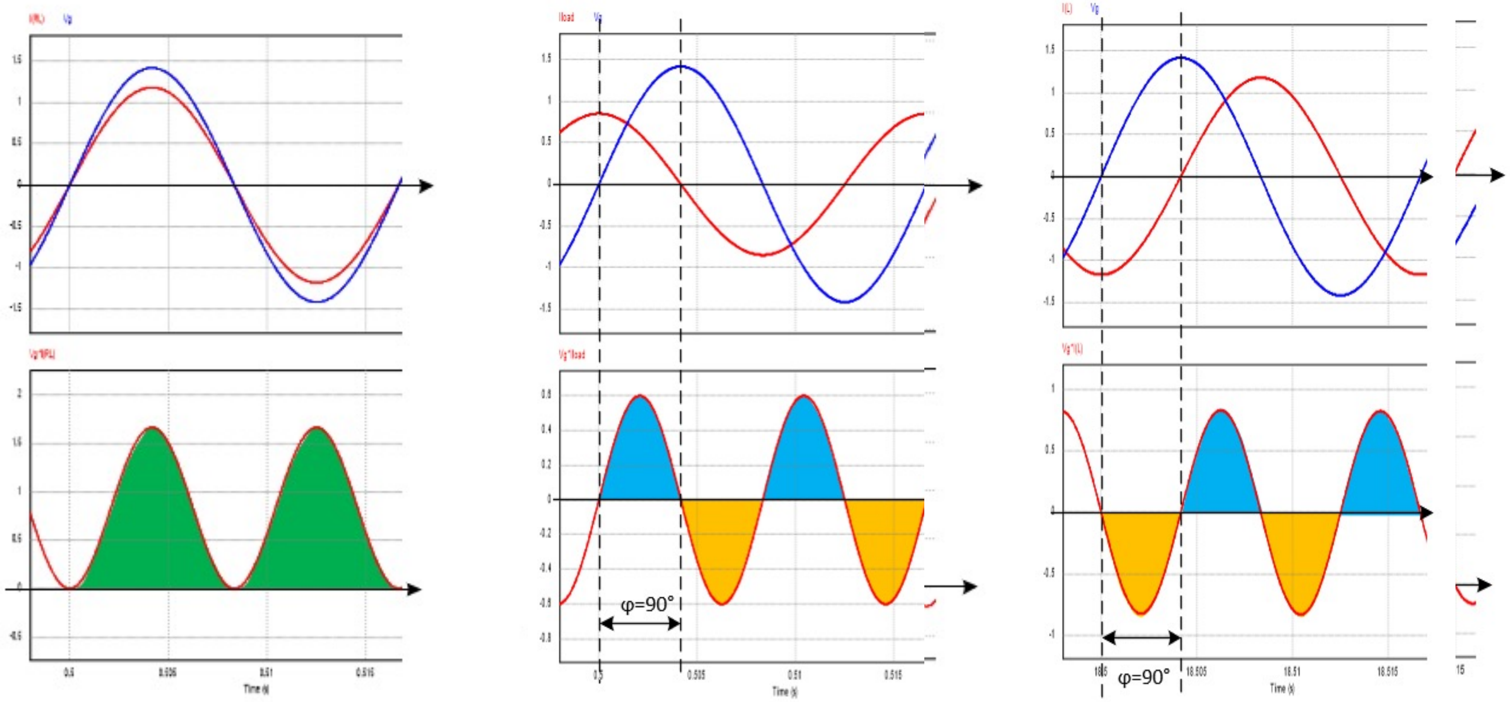
- Concept of PFC
- From Conventional PFC to Bridgeless Totem Pole PFC
- Digital Controlled Totem Pole Bridgeless PFC using Transphorm GaN and Microchip MCU

What is Power Factor?









$V_{grid} = \sqrt{2}V_s \sin(\omega t),$

where $V_s = 90\sim265V,$

$\omega = 2\pi f_o, f_o = 50\sim60Hz$

$i_{load} = \sqrt{2}I_s \sin(\omega t - \varphi)$

$\bar{P} = V_s I_s \cos\varphi$=Real Power

$S = V_s I_s$, Apparent power

The power factor:

$$PF = \frac{\bar{P}}{S} = \cos\varphi$$

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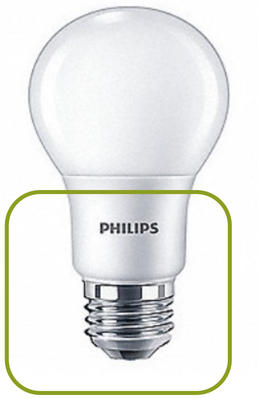
What are the real load and current?

MICROCHIP

40W Light Bulb

I1



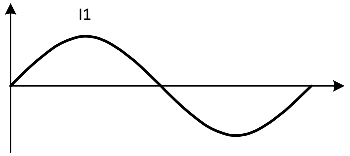
10W LED Bulb

I2

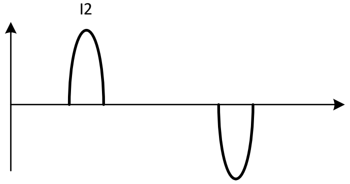
65W Laptop Power Supply

90W Laptop Power Supply

¼ HP Motor

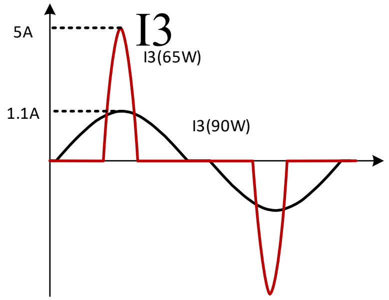


R

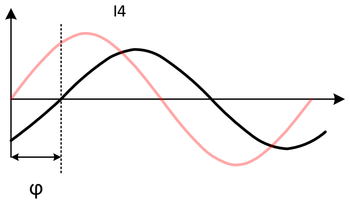


RCD

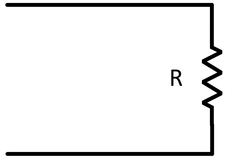
I3



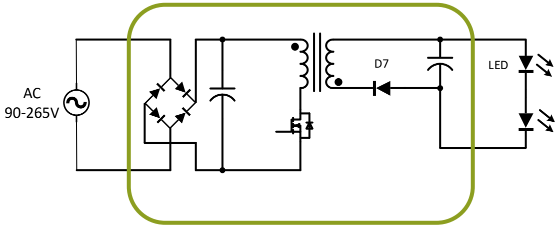
I4



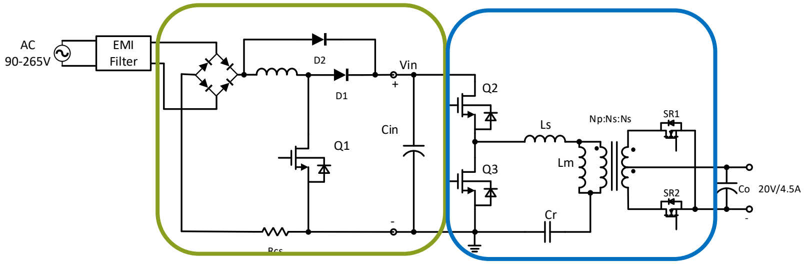
RL



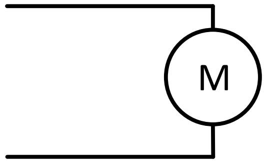
PF~1



Flyback, PF~0.75



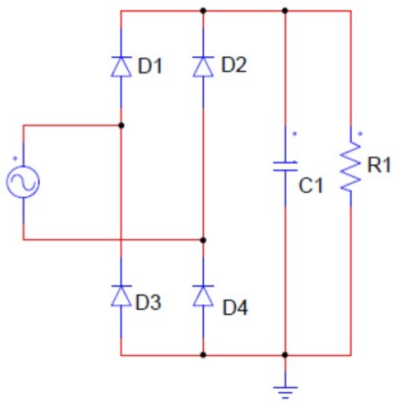
PFC + LLC, PF>0.95

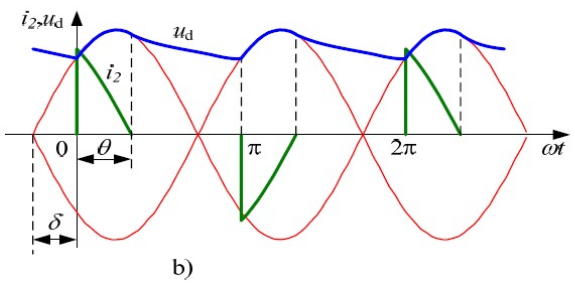


PF=0.6~0.8

Active PFC is necessary

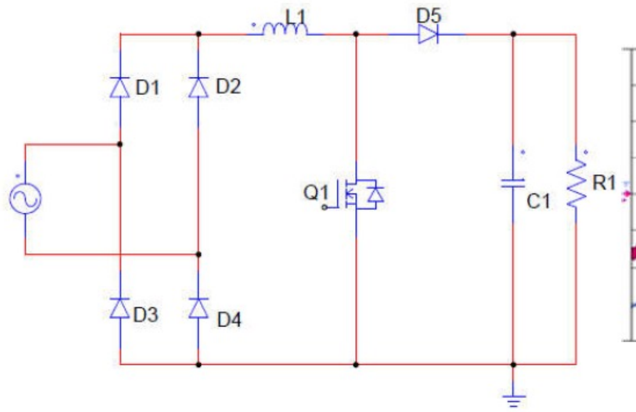
1, Why do we need PFC?
To mitigate the impact of harmonics and reduce the power loss, power factor correction is needed.
2, What is the goal of PFC?
To improve the power factor and reduce the harmonics current, so as to improve the power quality.
3, What is the basic topology of PFC?
The boost type converter is the basic circuit of PFC, as it has voltage boost function, and inductor connected to the grid is helping to improve the power quality.

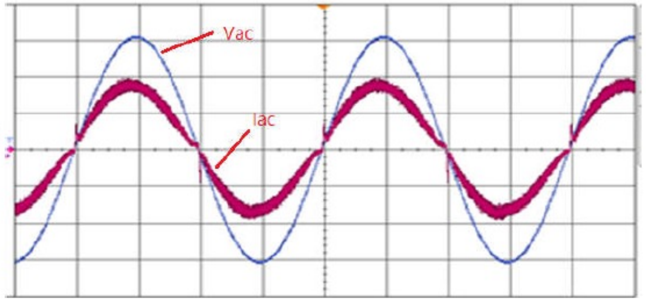




b)

PFC



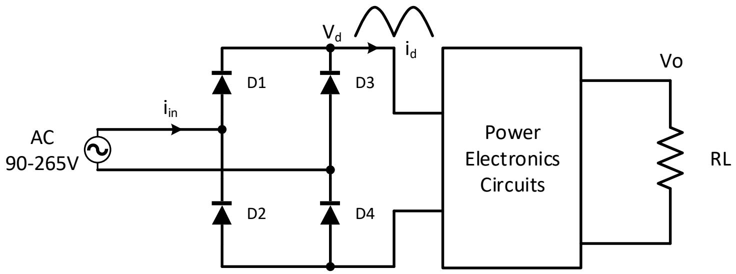


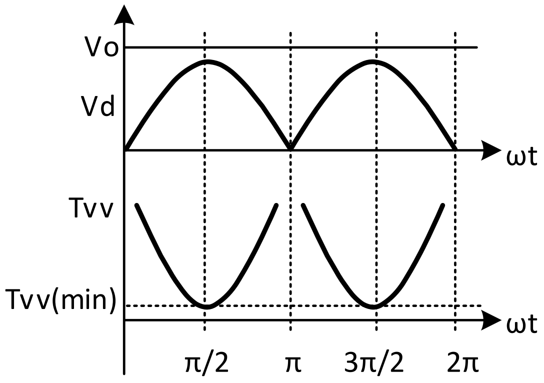
The basic power factor circuit

Basic Requirement:

For high power factor converter:

1. Keep ϕ=0, i.e. cosϕ = 1;
2. Reduce THDi, THDi < 5% (Meet IEC6100-3-2, IEEE-519)





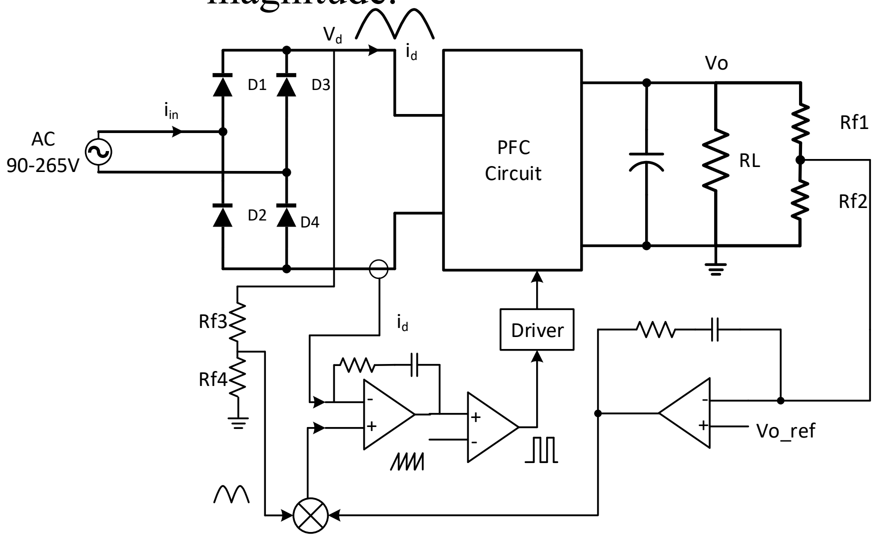
1, The output is the DC voltage with small ripples.
The voltage transfer ratio:

$$T_{vv}(\omega t) = \frac{v_o}{v_{in}(t)} = \frac{v_o}{v_d(t)} = \frac{V_o}{\sqrt{2}V_s|\sin(\omega t)|}$$

When $\omega t = k\pi + \pi/2$, $T_{vv}(\omega t)$ is minimum;
When $\omega t = k\pi$, $T_{vv}(\omega t) \to \infty$, need boost function
Converter to reduce the distortion at near zero-crossing:
Boost, Buck-boost, cuk, flyback, etc.
2, The input current $i_{in}(t)$ is in phase with $v_{grid}(t)$:

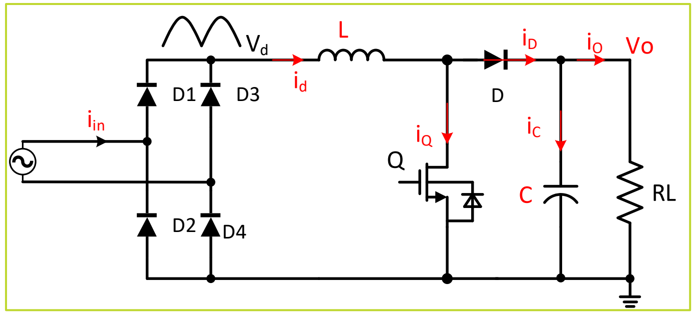
$$i_{in}(t) = A \cdot V_s|\sin(\omega t)|$$

3, Output voltage is controllable by adjusting the input current magnitude.

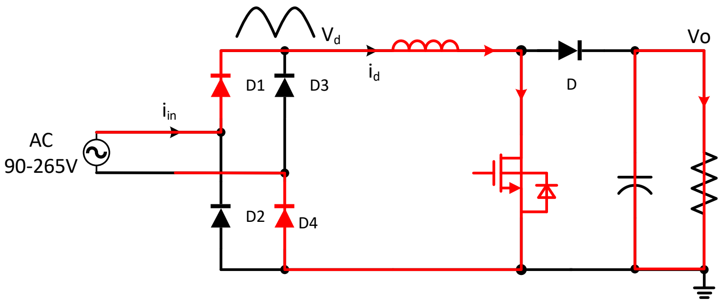


Basic Control Diagram

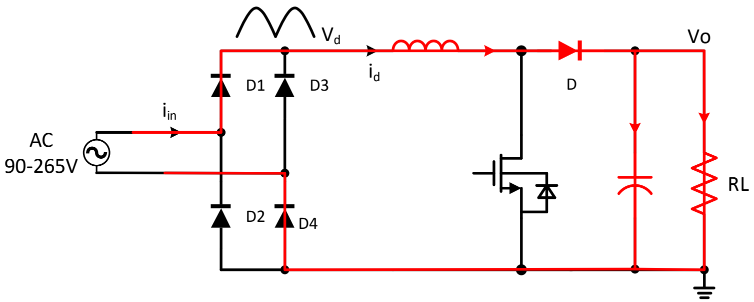
Traditional Diode Bridge Boost PFC

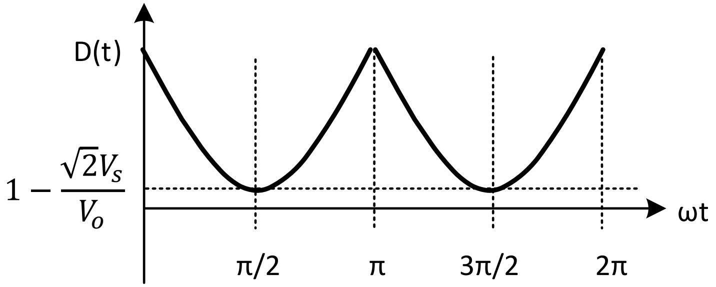


Stage I: switch Q is on.
Inductor is charging



Stage II: switch Q is off.
Inductor is discharging



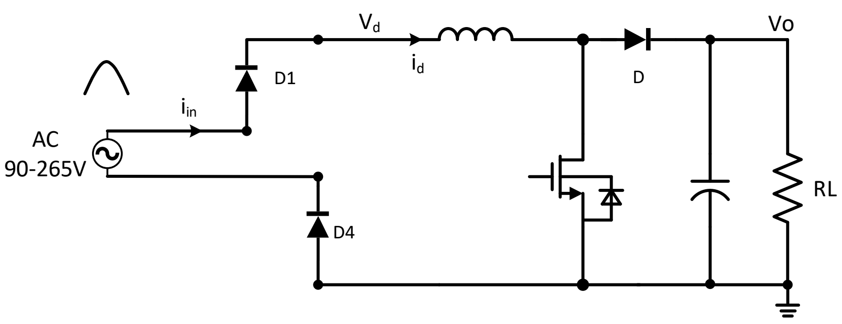


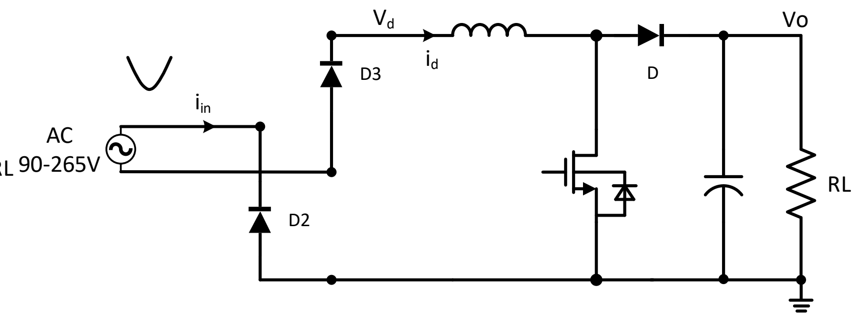
1, The output is the DC voltage with small ripples. Boost function to reduce the distortion at near zero-crossing.
2, The input current $i_{in}(t)$ is in phase with $v_{grid}(t)$: $i_{in}(t) = A \cdot V_s|\sin(\omega t)|$
3, Output voltage is controllable by adjusting the input current magnitude.

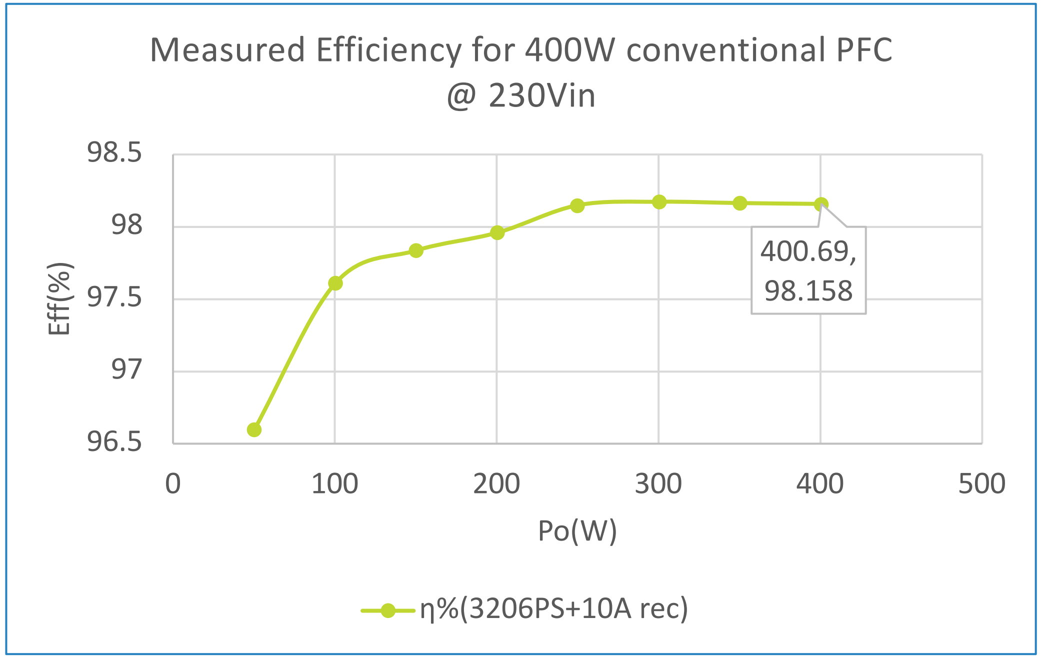
Duty cycle of a boost PFC converter: in one switching cycle, the average voltage on inductor is zero:

$$D(t) = 1 - \frac{\sqrt{2}V_s|\sin(\omega t)|}{V_o}$$

Issues on Diode Bridge PFC: Low Efficiency







Two rectified diodes are always connected in series in the circuit,

For a 230V/400W power supply as an example:

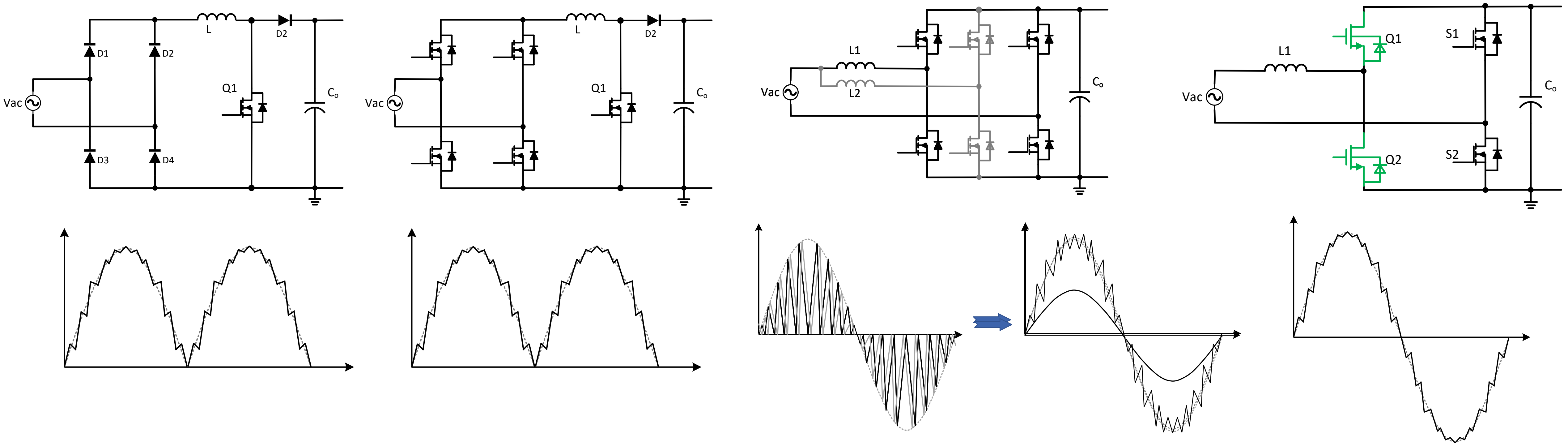
$$P_{con\_D1,2} = 2\frac{2\sqrt{2}}{\pi}I_sV_f = \frac{2\sqrt{2}}{\pi}\times 1.77A\times 1V = 3.19W$$

$\frac{3.19W}{400W}\times 100\% = 0.8\%$ efficiency loss in the rectified diode bridge.

At low line condition, the loss will be doubled.

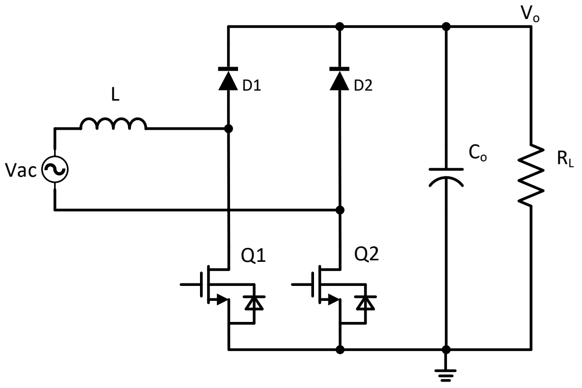
If the conduction loss is saved, the efficiency could be 99% at high line.

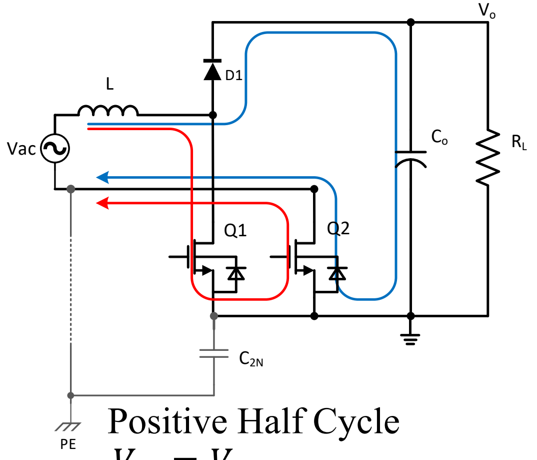
AC-DC PFC Converter



Topology	Diode Bridge Boost PFC	MOSFET Bridge Boost PFC	CRM Bridgeless Totem Pole PFC		CCM Bridgeless Totem Pole PFC
			Single Leg	Interleaved	
Efficiency (high line)	98.2%	98.8%	99 %	> 99%	> 99%
Power level	Mid	Mid to High	Low	Mid	High
Issue	High Power Loss	Low Surge Tolerance	High EMI	Complex Ctrl	
Components Count	Mid	Very High	Low	High	Low

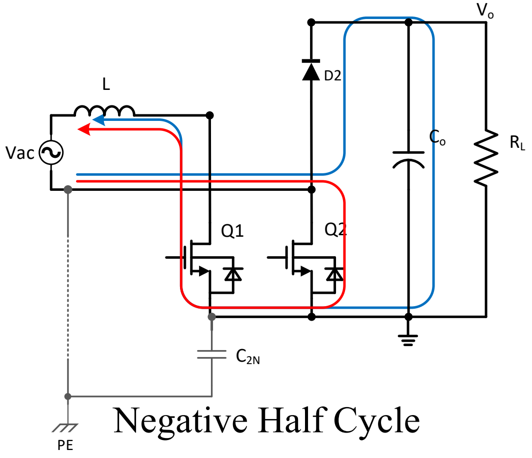
Bridgeless PFC Topology I





Positive Half Cycle

$V_{gn} = V_{PGND}$



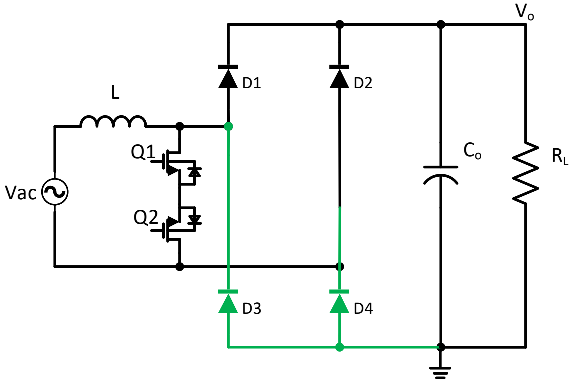
Negative Half Cycle

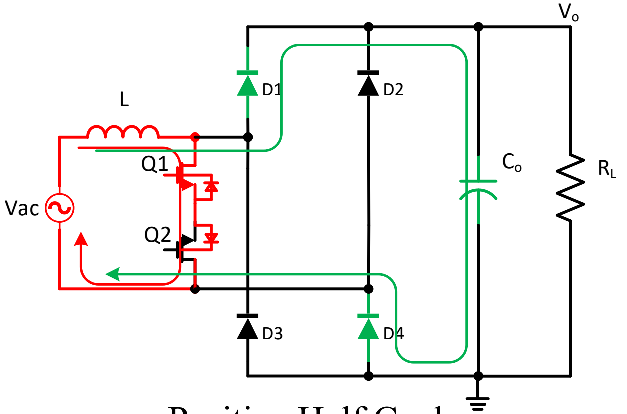
$V_{gn} = V_{PGND}(Q2\ is\ on)$

$V_{gn} = V_o(D2\ is\ conducting)$

At positive half cycle, Vgn is constant and there is no common mode noise;
At negative half cycle, Vgs is switching between V_{PGND} and V_o , common mode noise will be seen.

Adding diodes on DC side

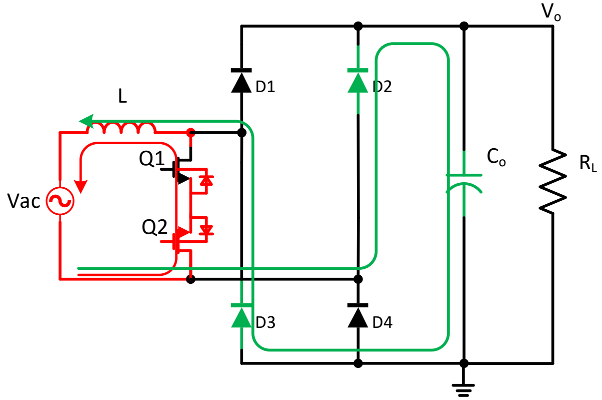




Positive Half Cycle

$V_{gn} = \frac{V_o}{2}$ ($Q1\ on$)

$V_{gn} = V_{PGND}$ ($D1, D4\ conducting$)



Negative Half Cycle

$V_{gn} = \frac{V_o}{2}$ ($Q2\ on$)

$V_{gn} = V_o$ ($D2, D3\ conducting$)

When active switching Q is on, Vgn is Vo/2, when diodes are conducting, Vgn is tie to GND or Vo. The votlage change reduces from Vo to Vo/2

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Bridgeless PFC Topology II

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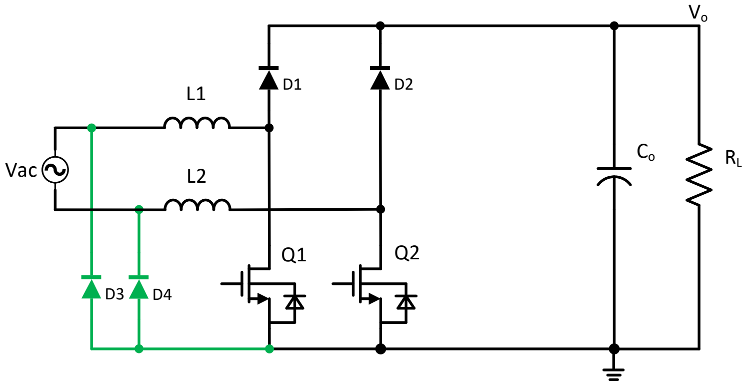
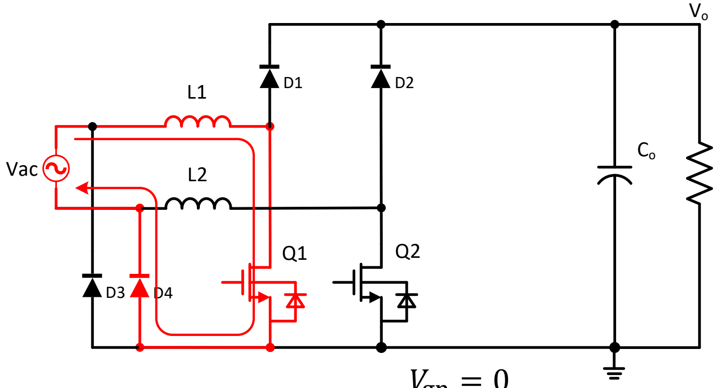
Add two diodes D3, D4 on AC side and one more inductor.



No common mode noise issue.

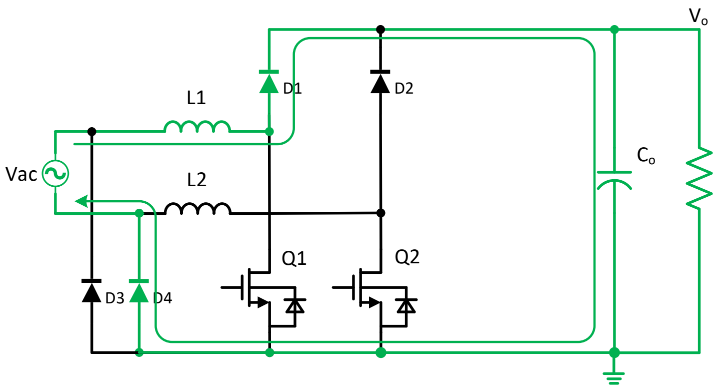
In Positive half cycle

Q1 is on



$V_{gn} = 0$

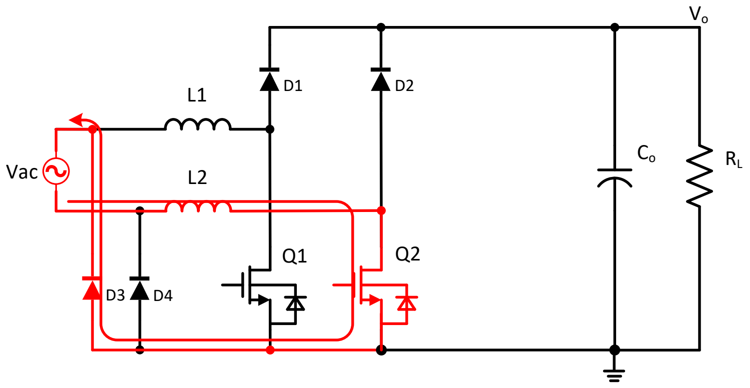
Q1 is off



$V_{gn} = 0$

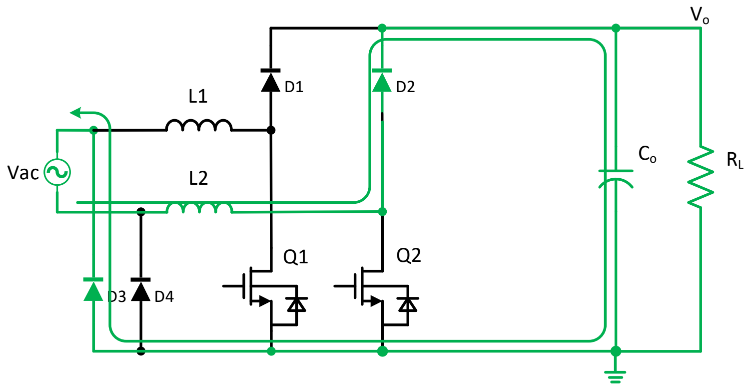
In Negative half cycle

Q2 is on



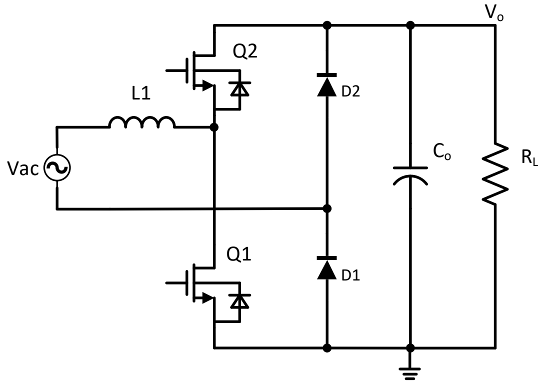
$V_{gn} =- V_{ac}$

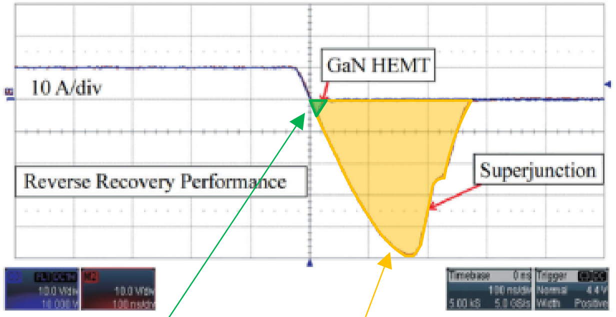
Q2 is off



$V_{gn} =- V_{ac}$

Bridgeless PFC Topology IV-Totem Pole PFC



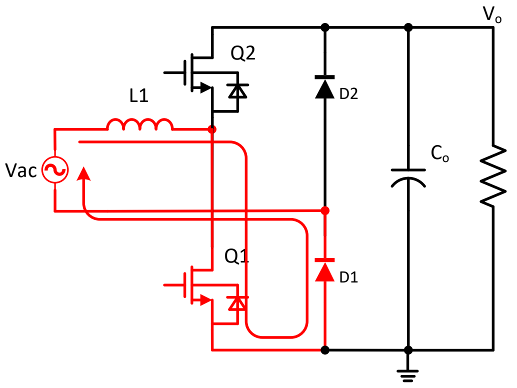


Parameter	TP65H035G4WS	IPB60R040CFD7
ID	46.5 A (Continuous)	50 A (for D=0.75)
Ron	41 mΩ	40 mΩ
Qg	22 nC	108 nC
Eoss(400V)	17 uJ	12.5 uJ
Qrr	150 nC (1A/ns)	1.76 uC (0.1A/ns)

Table 1: Comparison of GaN HEMT with equivalent CoolMOS IPB60R040CFD7

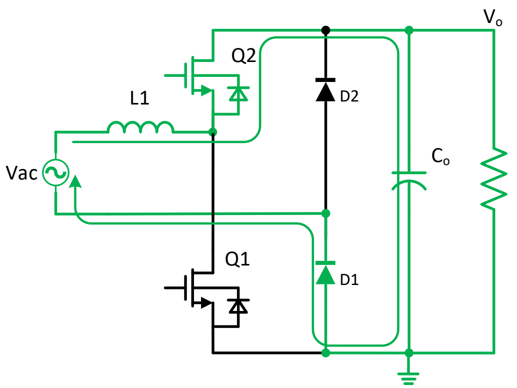
In Positive half cycle

Q1 is on



$V_{gn} = V_{PGND}$

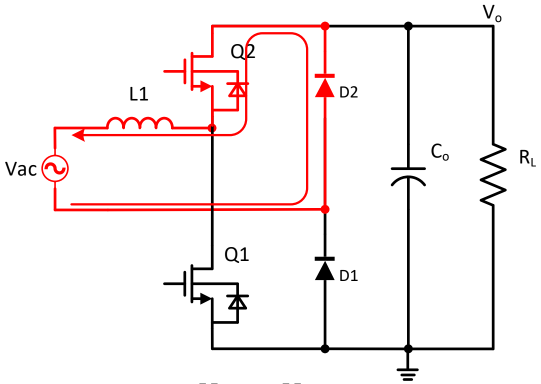
Q1 is off



$V_{gn} = V_{PGND}$

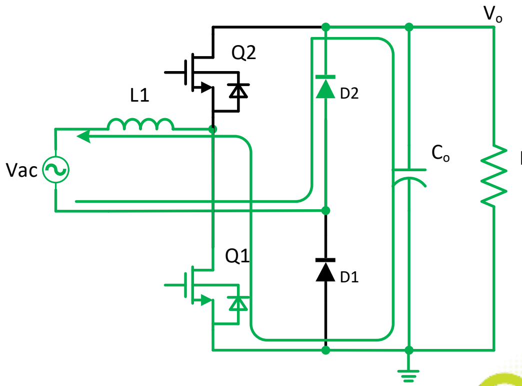
In Negative half cycle

Q2 is on



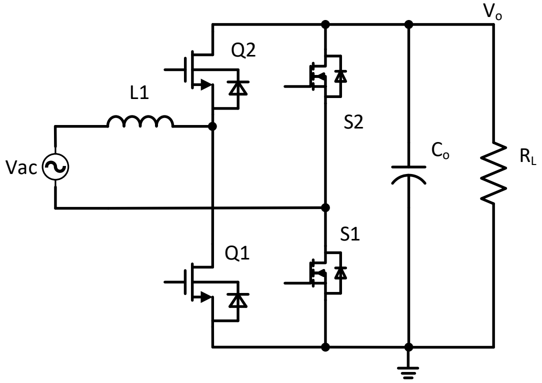
$V_{gn} = V_O$

Q2 is off



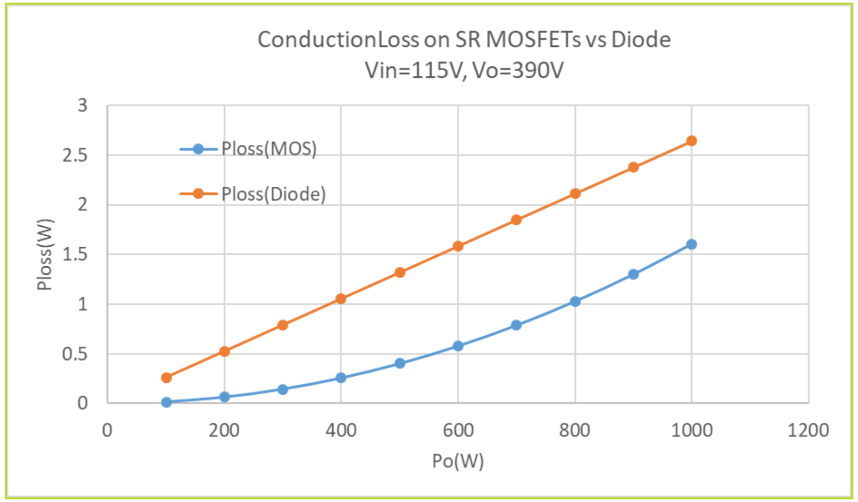
$V_{gn} = V_O$

Improvement-using synchronous MOSFETs

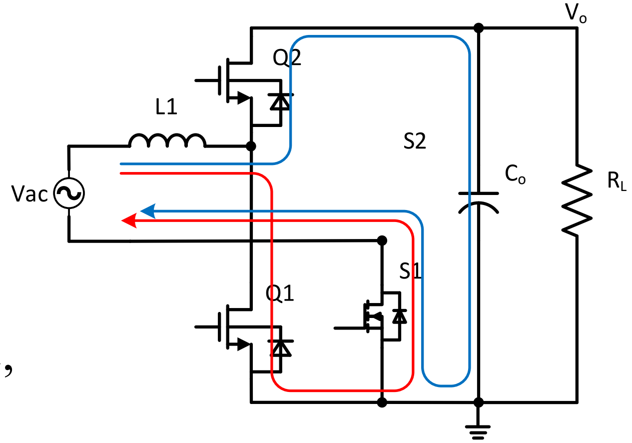


D1, D2 are replaced by MOSFETs S1 and S2, The conduction loss is reduced.

Vf_Diode=1V, Rds(on)_MOSFET=20mΩ

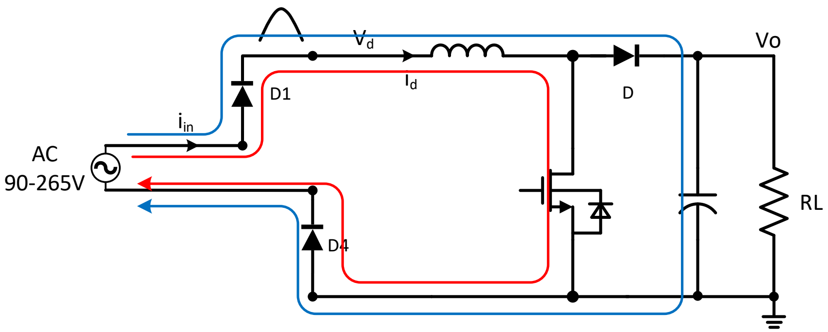


Totem Pole PFC



Q1 is on: Q1, S1 conducting
Q1 is off: Q2, S1 conduction
No Diode Vf drop.

Conventional Diode Bridge PFC



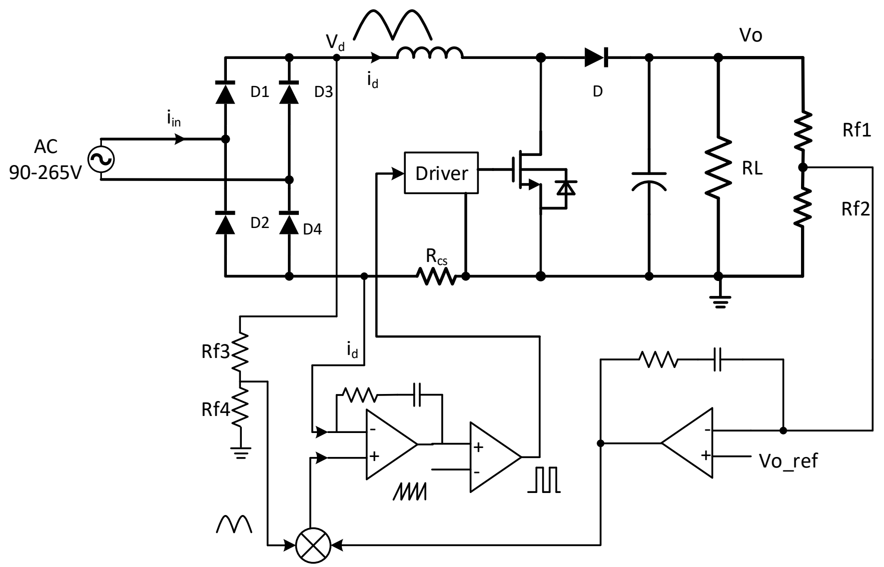
Q1 is on: D1, Q1, D4 conducting
Q1 is off: D1, D4, D conducting

Hardware design overview and Challenges

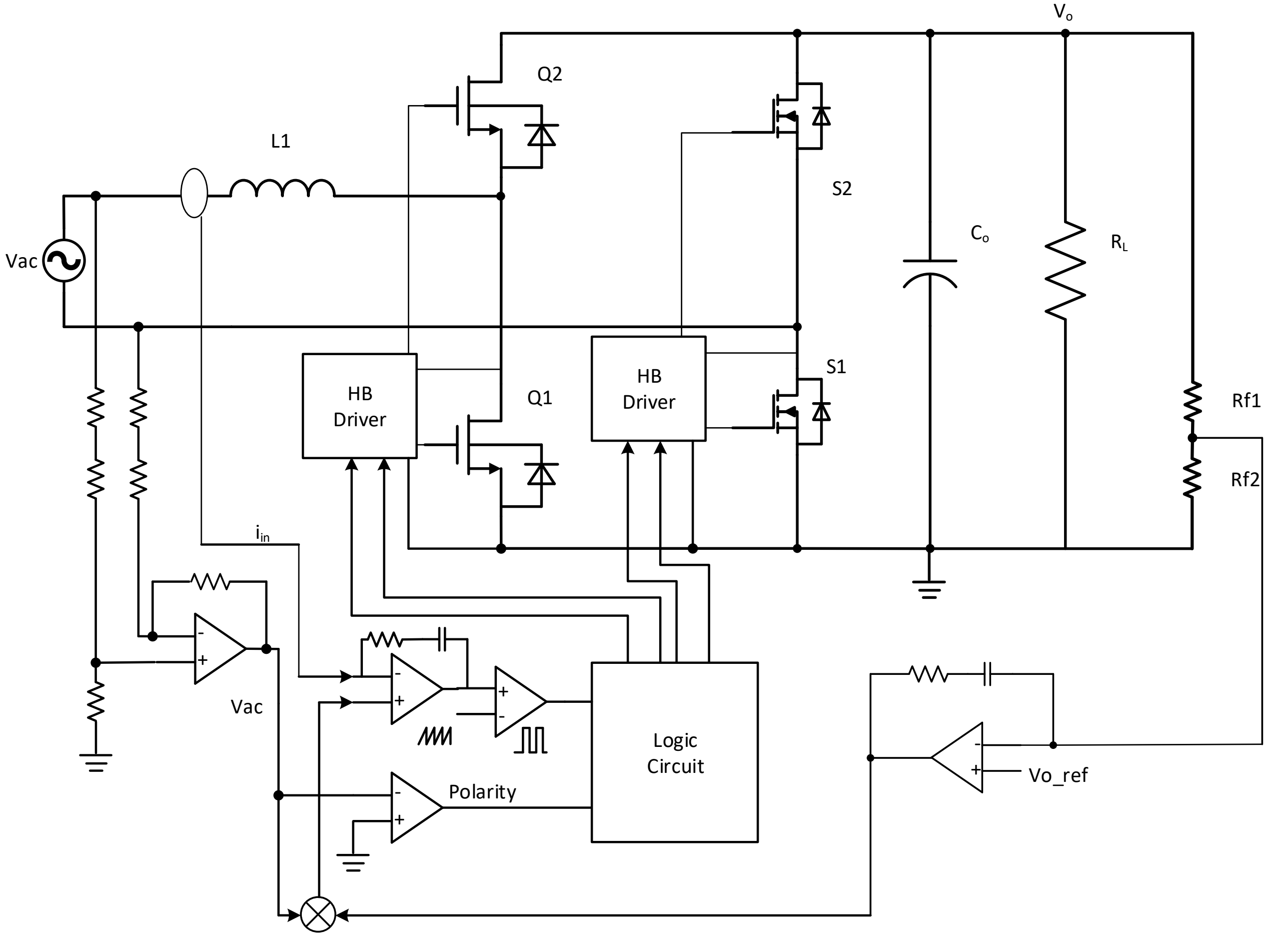
- 1. Input voltage sensing, AC polarity detection
- 2. Input current and DC bus voltage sensing
- 3. GaN HEMT and SR MOSFET power stage
- 4. Inrush thermistor at Start-up
- 5. DSP control card interface

Design Challenge for Totem Pole PFC

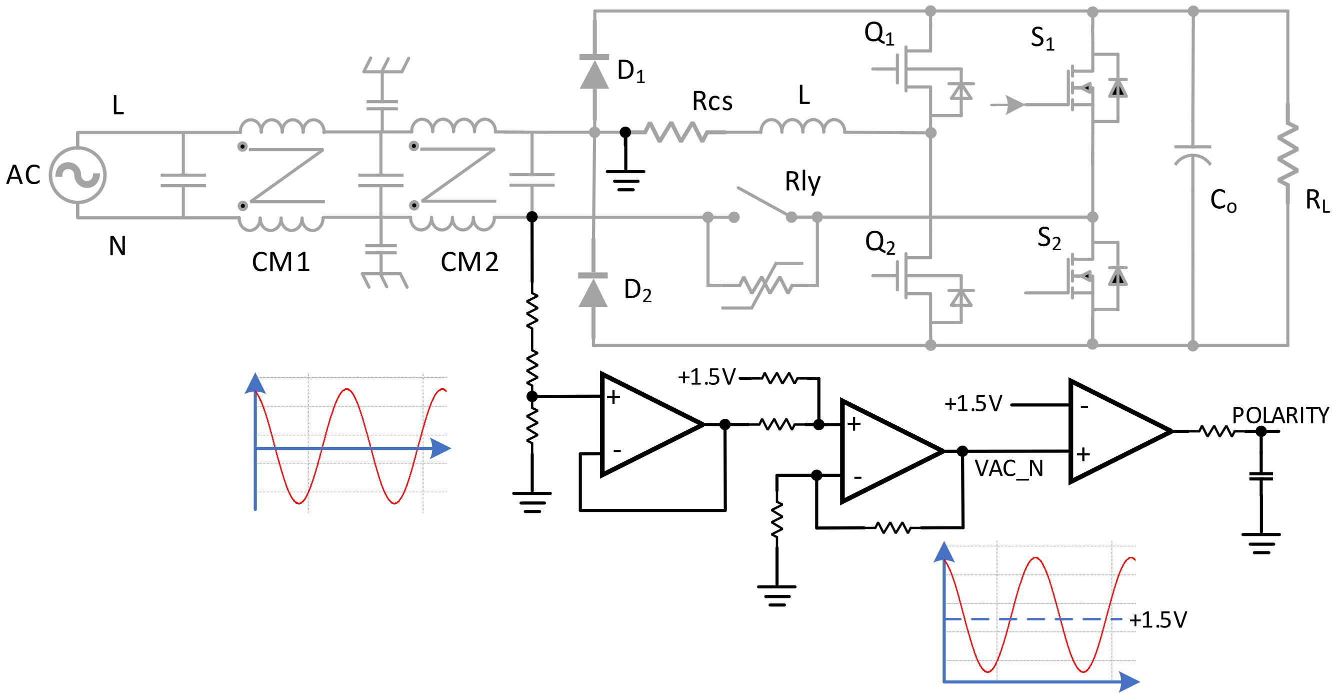
Control and driving circuit for traditional PFC



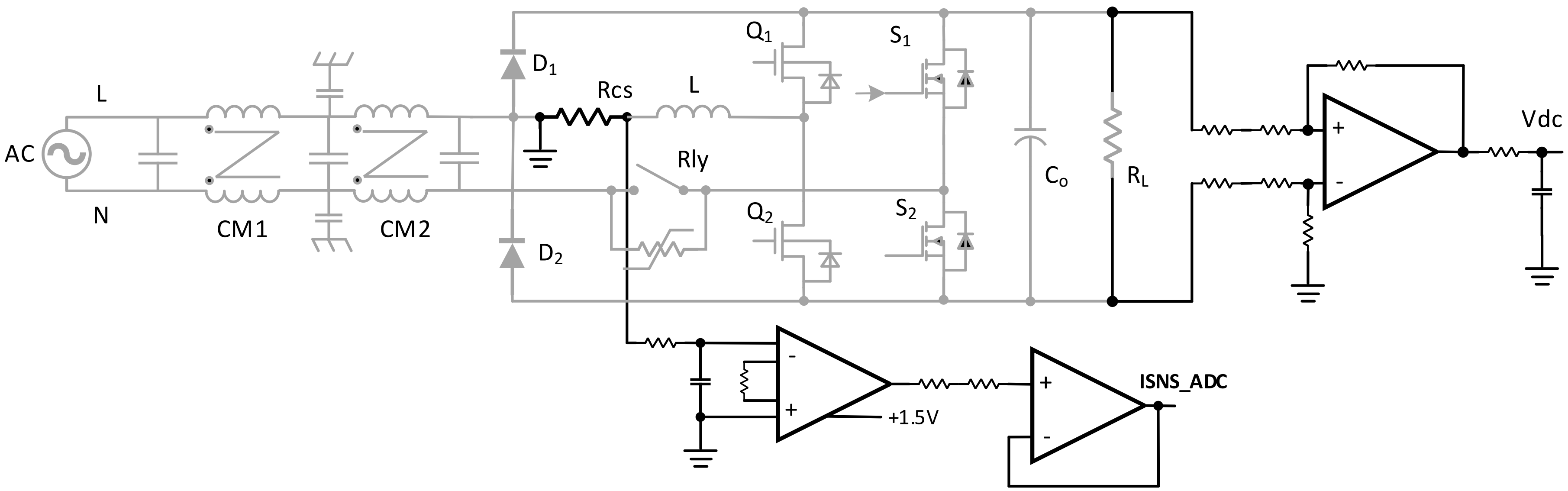
Control and driving circuit for Totem Pole PFC



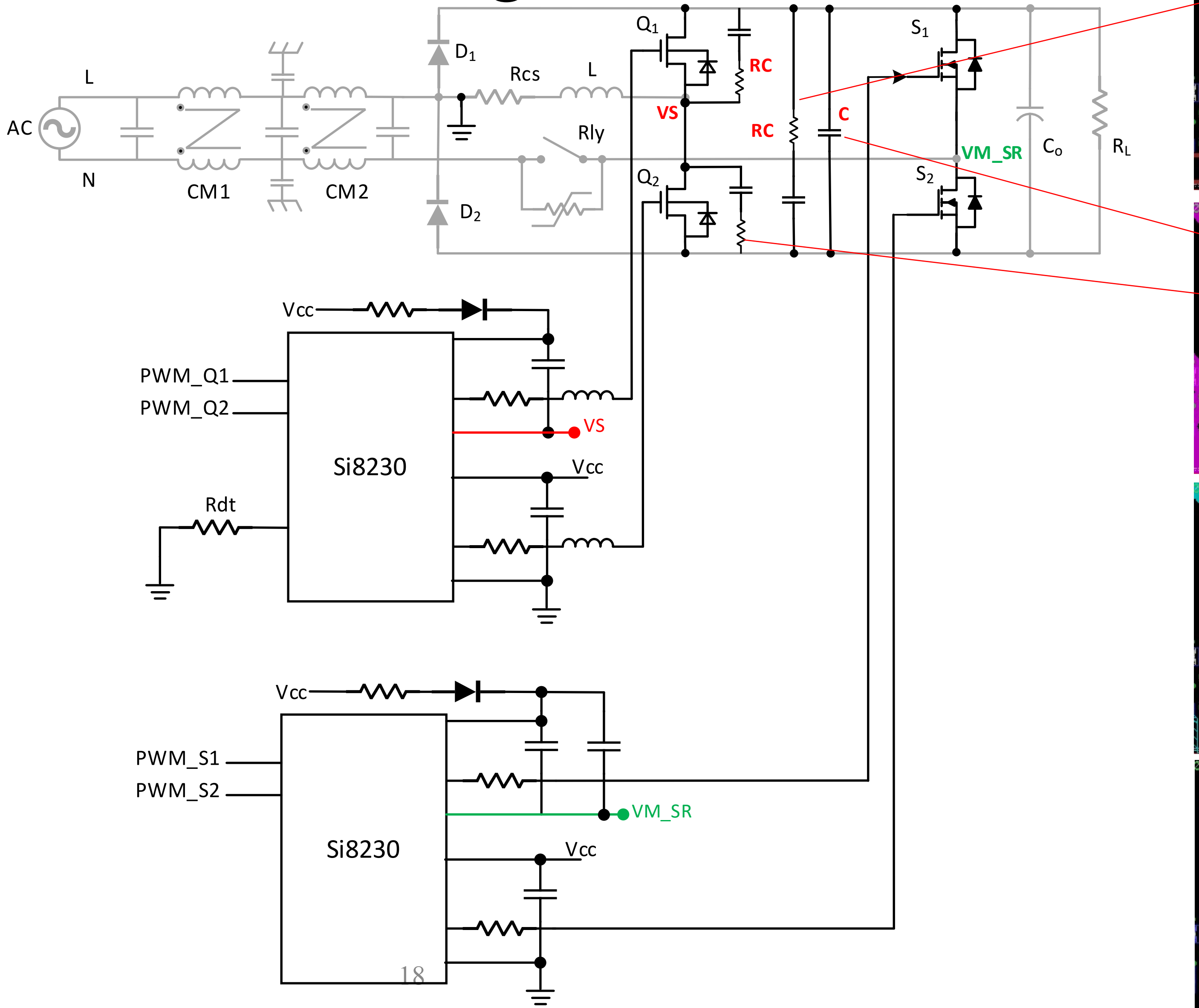
1. Input voltage sensing, AC polarity detection

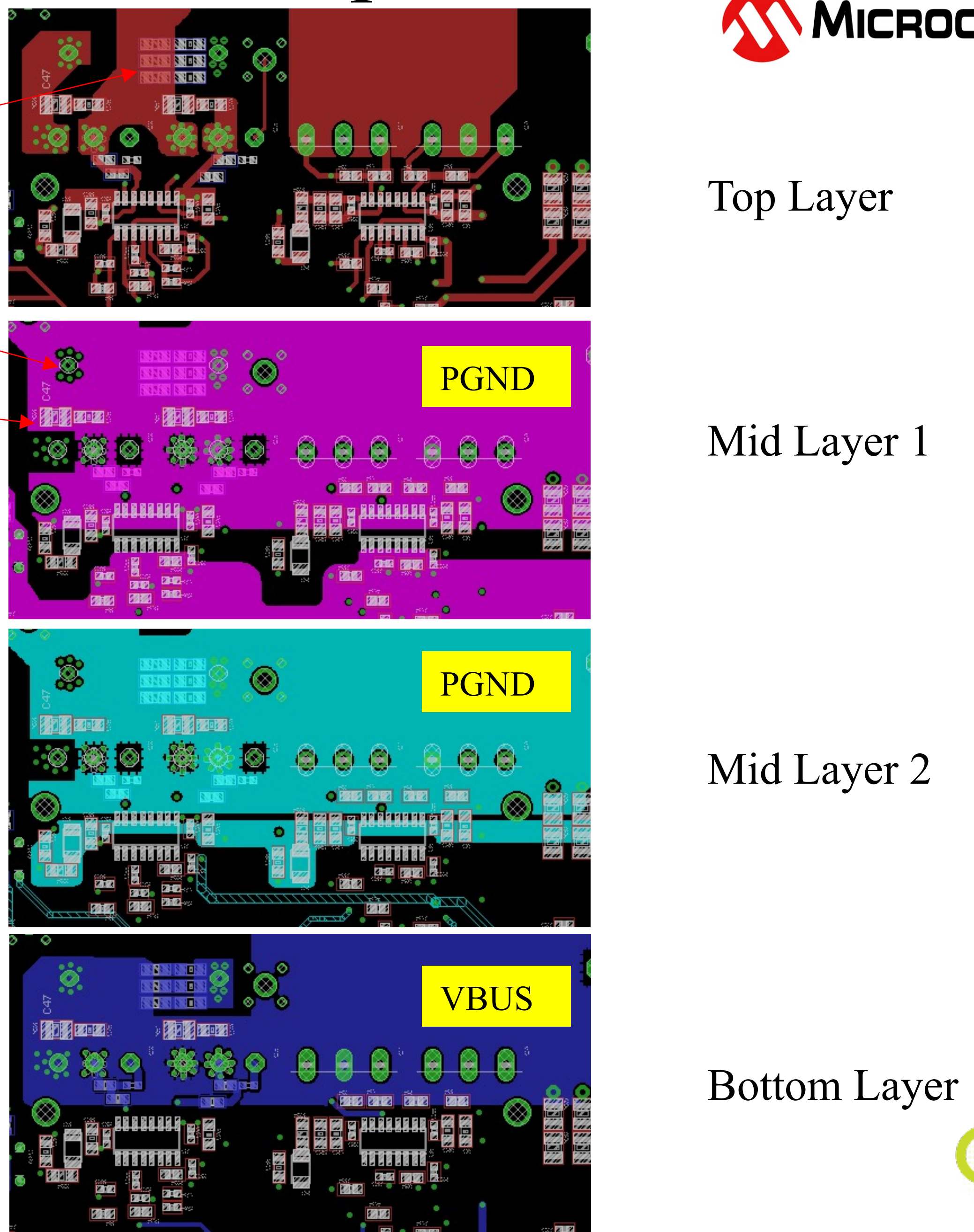


2. Input current and DC bus voltage sensing



3. GaN HEMT and SR MOSFET power stage





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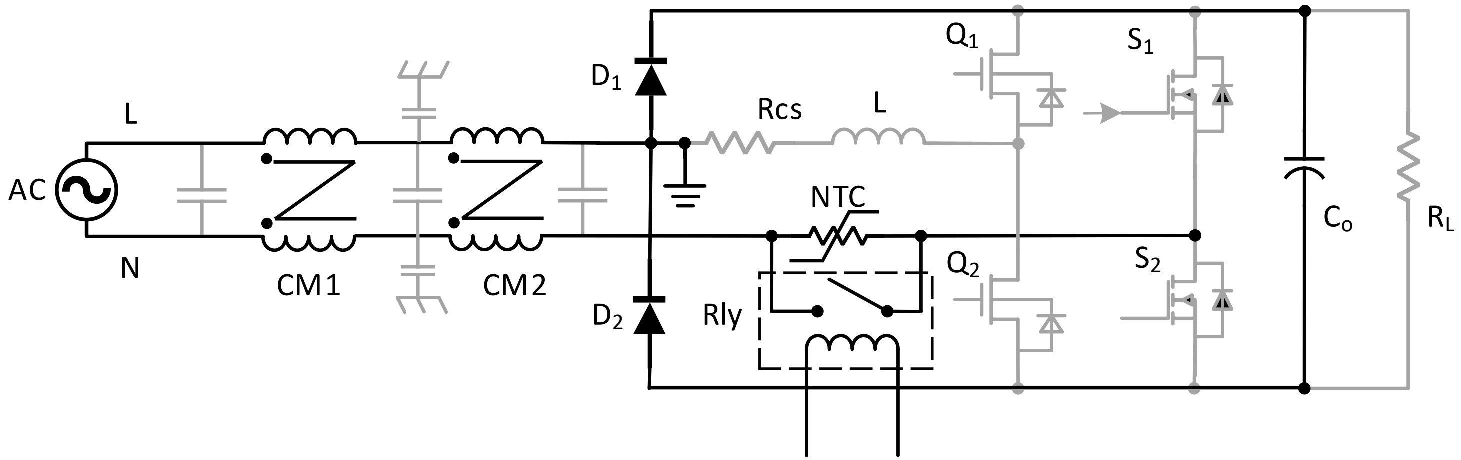
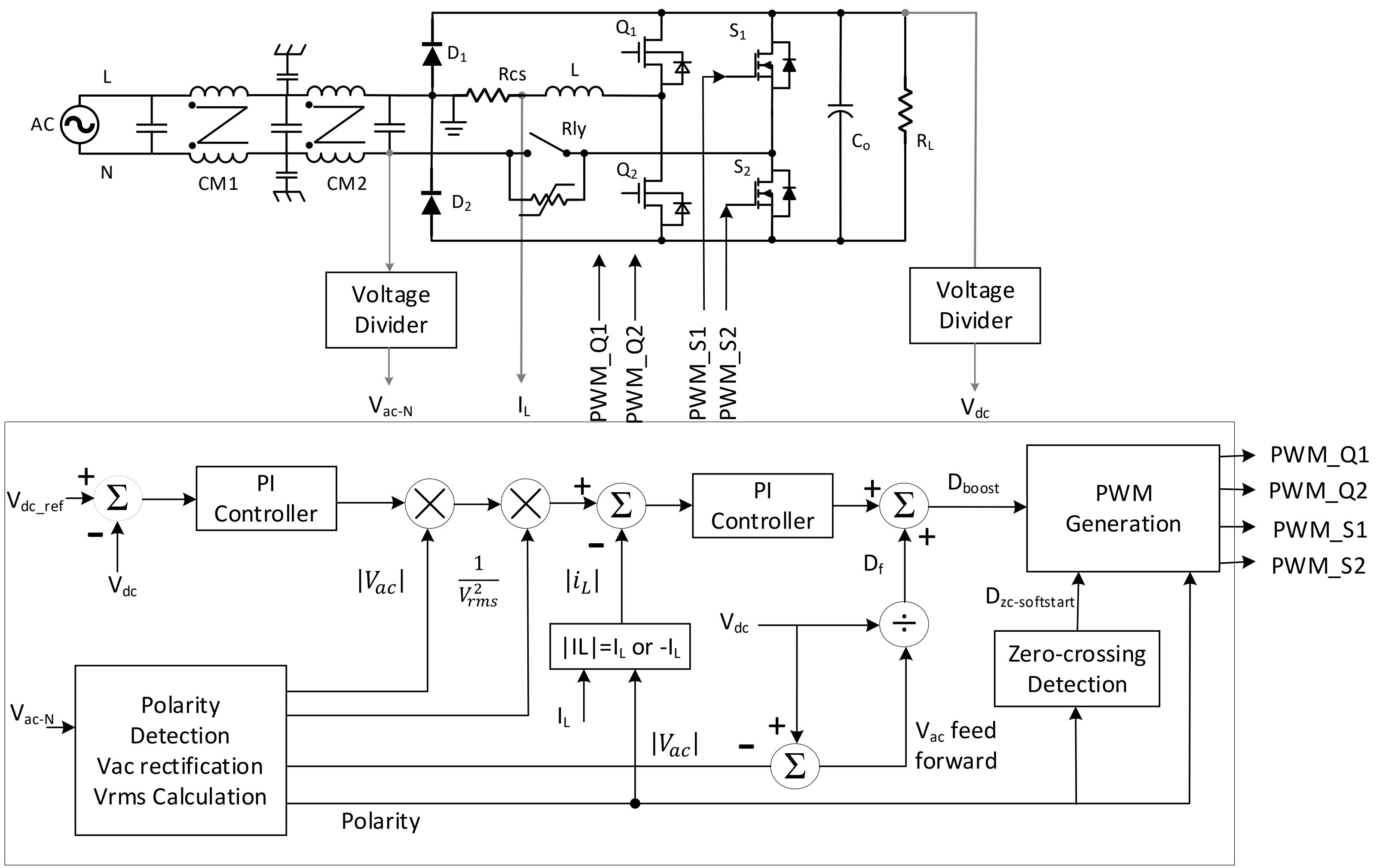
4. Inrush thermistor and bypass Diode at Start-up

MICROCHIP



1, When AC grid voltage is connected, DC bus capacitor will be pre-charged through NTC and D1, D2;
2, Relay is closed to bypass the NTC, and DC bus voltage increases to peak of the grid voltage;
3, PFC controller start to work. Q1 and Q2 will operate in PWM mode at positive half cycle.

5. DSP control card interface



Totem Pole PFC using Trasphorm GaN FETs

4 kW Bridgeless Totem-Pole: TDTTP4000W066C

Transphorm SuperGaN™ and Microchip dsPIC33CK

Test Setup and Conditions	
Evaluation Kit	TDTTP4000W066C-KIT
Operating frequency	66 kHz
Input voltage	85 V_{ac} to 265 V_{ac}
Output voltage	387 V_{dc} ±5 V_{dc} (programmable)
Digital power PIM	dsPIC33CK256MP506
GaN device	TP65H035G4WS
Gate resistor	30 Ω
Gate ferrite bead	200 Ω @ 100MHz
Snubber circuit	Not required
Deadtime	Programmable

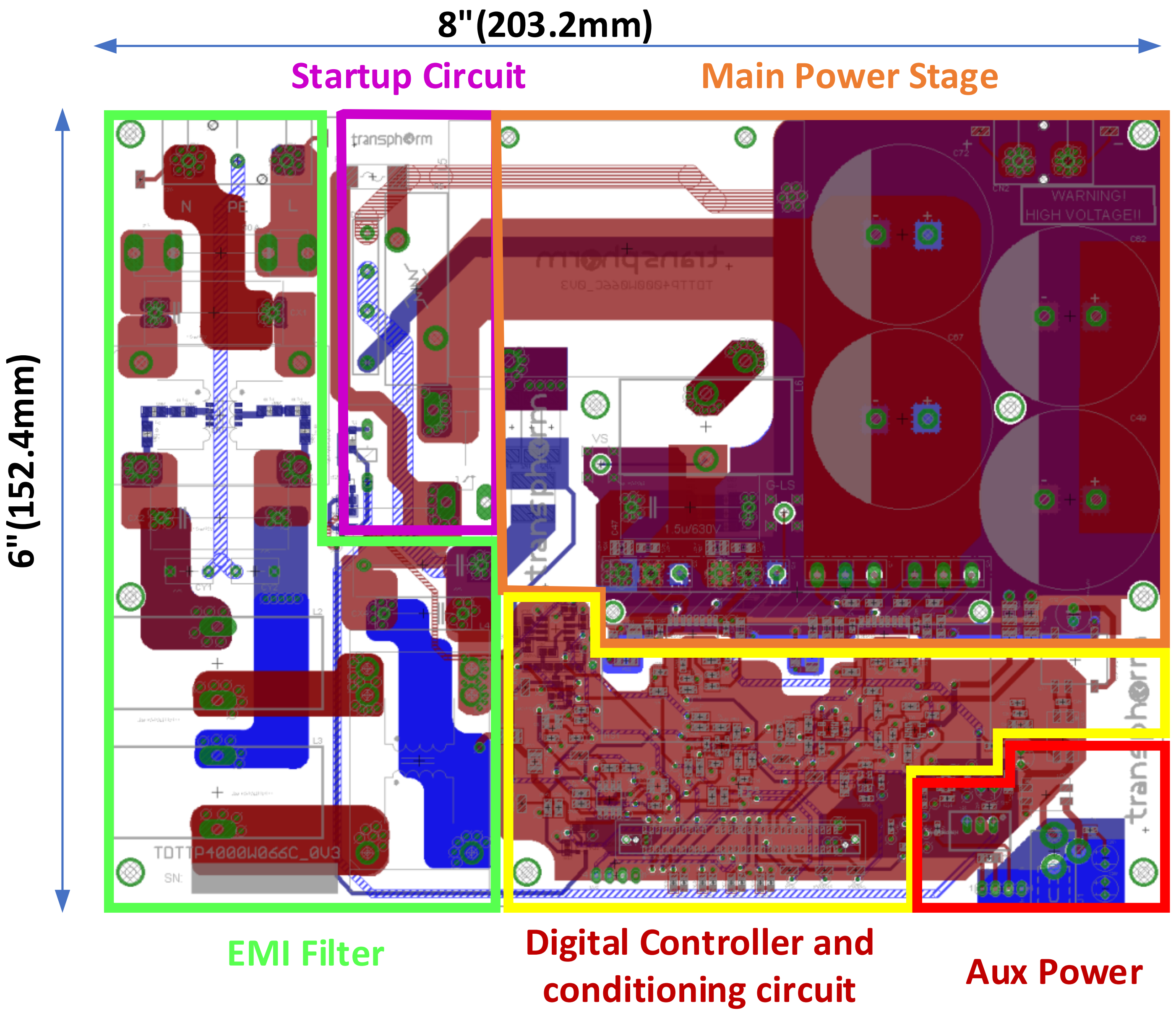
Digital Controller: Microchip dsPIC33CK

Available at:

transphorm

PCB Layout

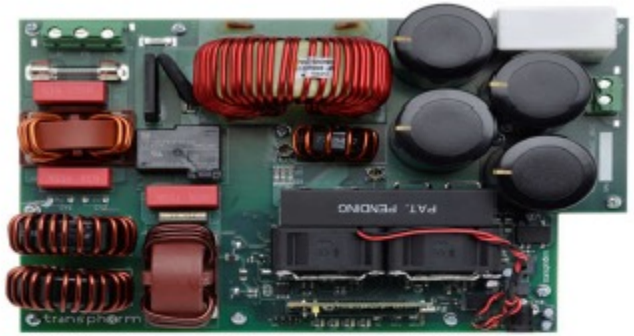
MICROCHIP

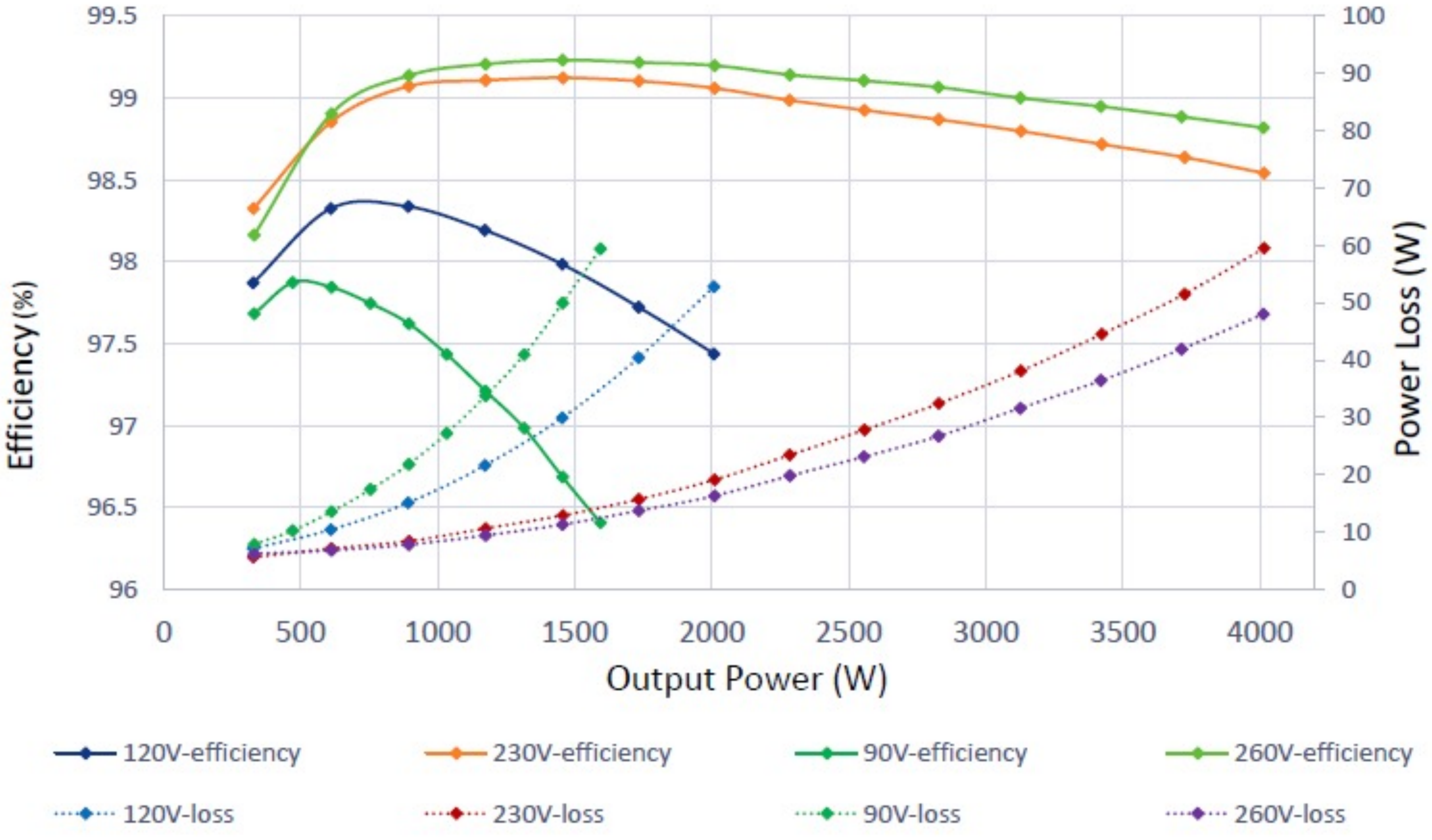


Totem Pole PFC using Trasphorm GaN FETs

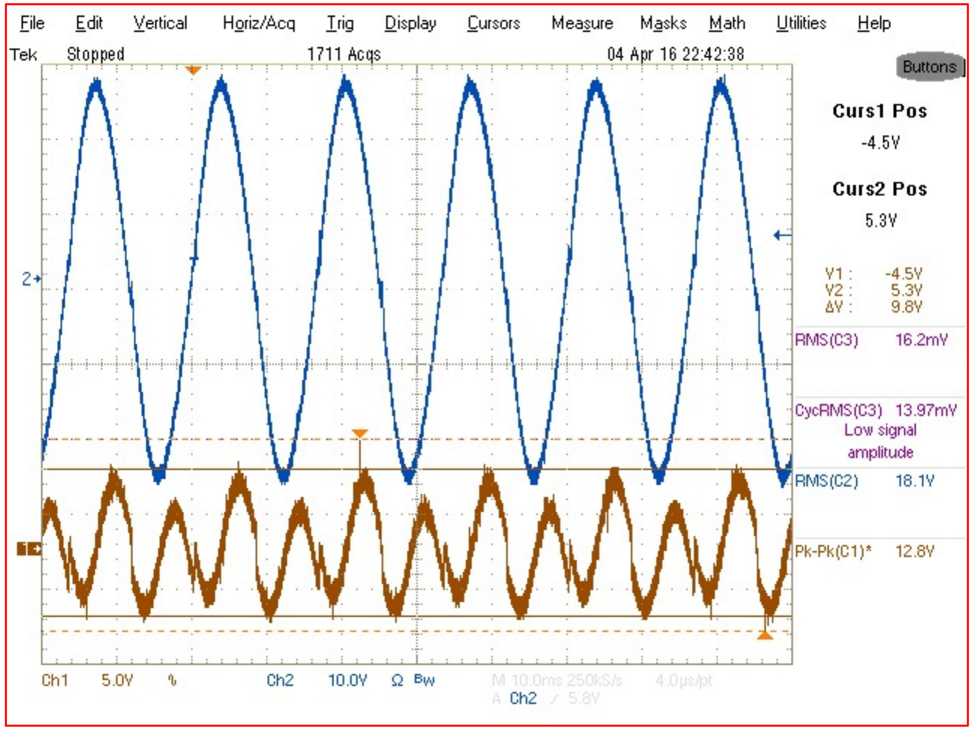
4 kW Totem-Pole Efficiency Sweep Results

Transphorm SuperGaN™ and Microchip dsPIC33CK

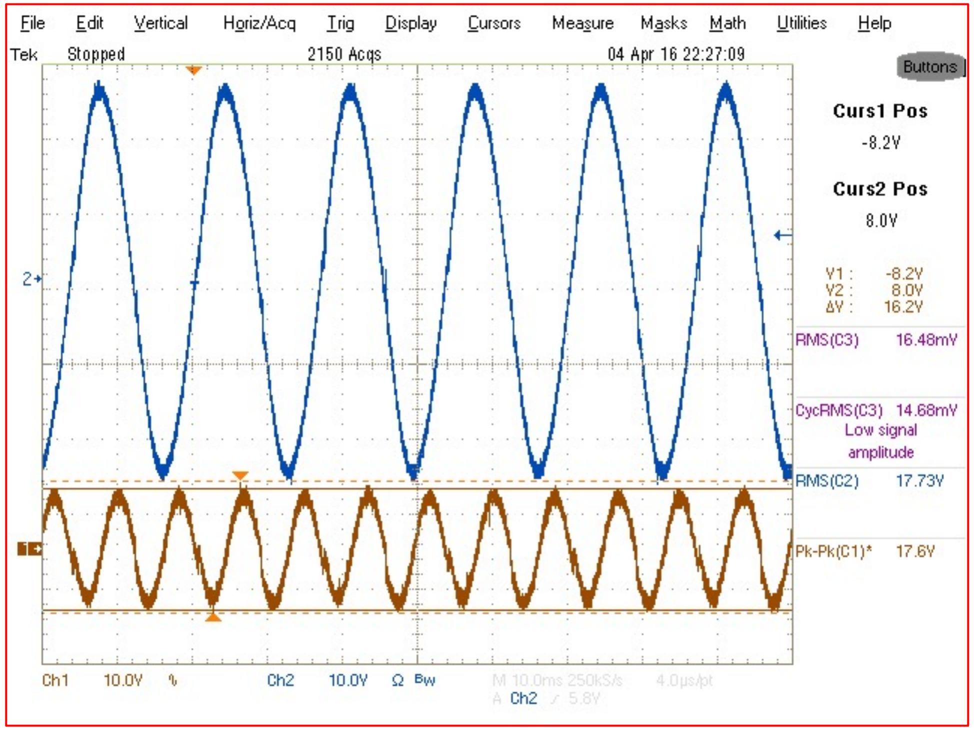




Vo ripples @ full load



Low line 115V, 2kW full load



High line 230V, 4kW full load

Co=2250uF;
T_holdup=15ms;
$\Delta V < 5\%Vo = 19.3V$

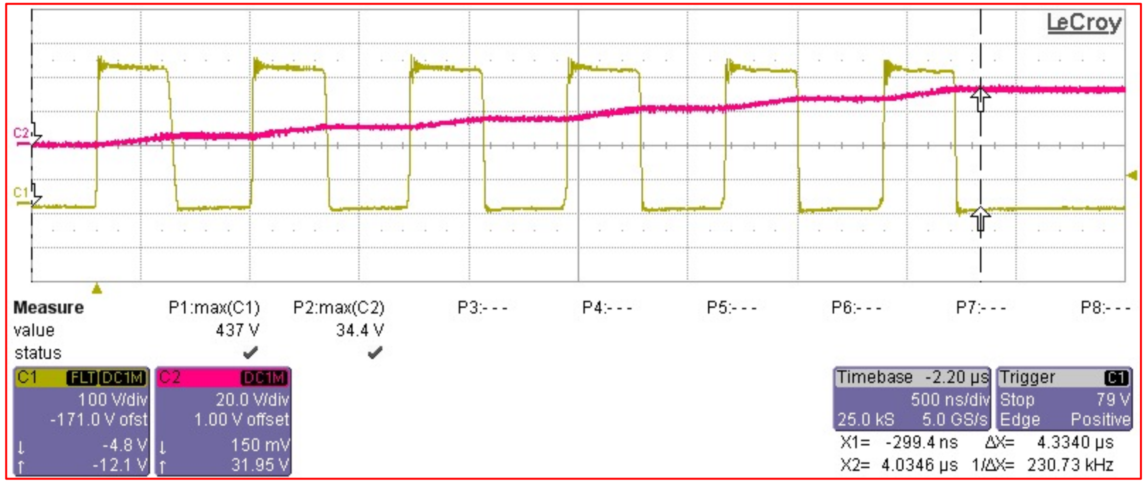
$i_{co_{rms}} = 10.434A\ (4kW)$

4x 470uF, 2.82A Capacitors.

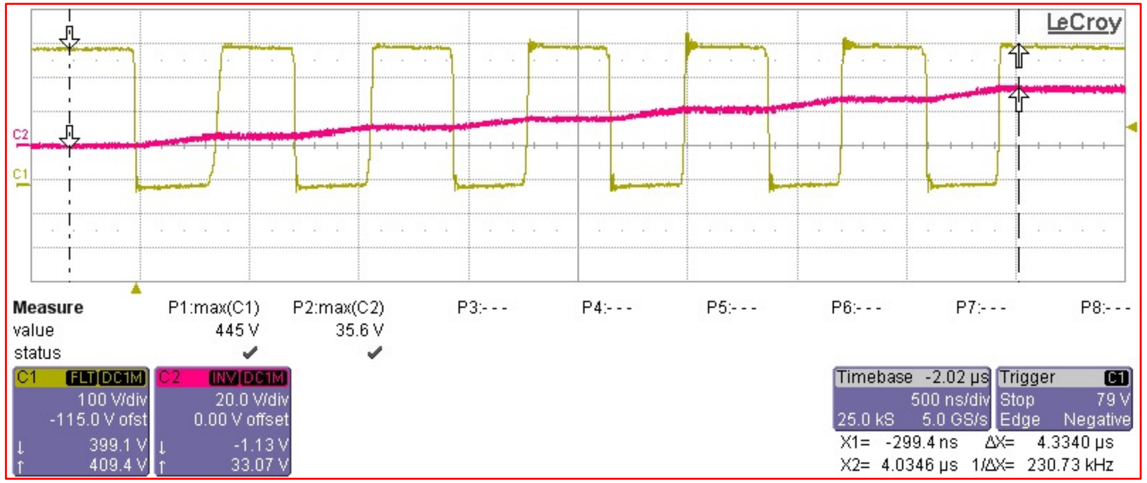
CH1: Iin_rms = 18.1A
CH2: Vo_ripple = 9.8V (2.5%)
Vo_ripple+noise = 12.8V

CH1: Iin_rms = 17.7A
CH2: Vo_ripple = 16.2V (4.2%)
Vo_ripple+noise = 17.6V

Voltage on GaN device

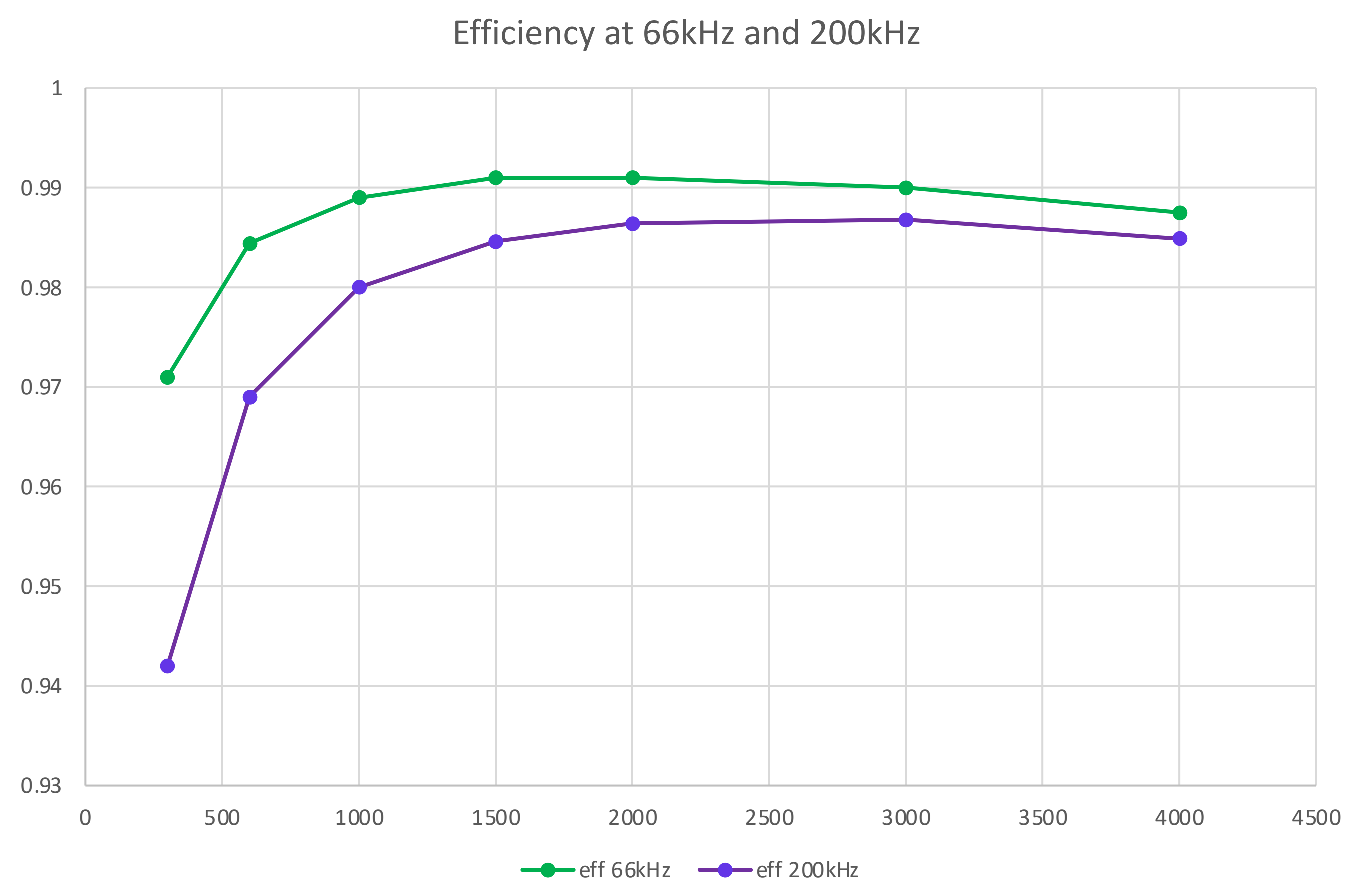


High Side switch to 34.4A



Low Side switch to 35.6A

Estimated Efficiency with 200kHz Switching



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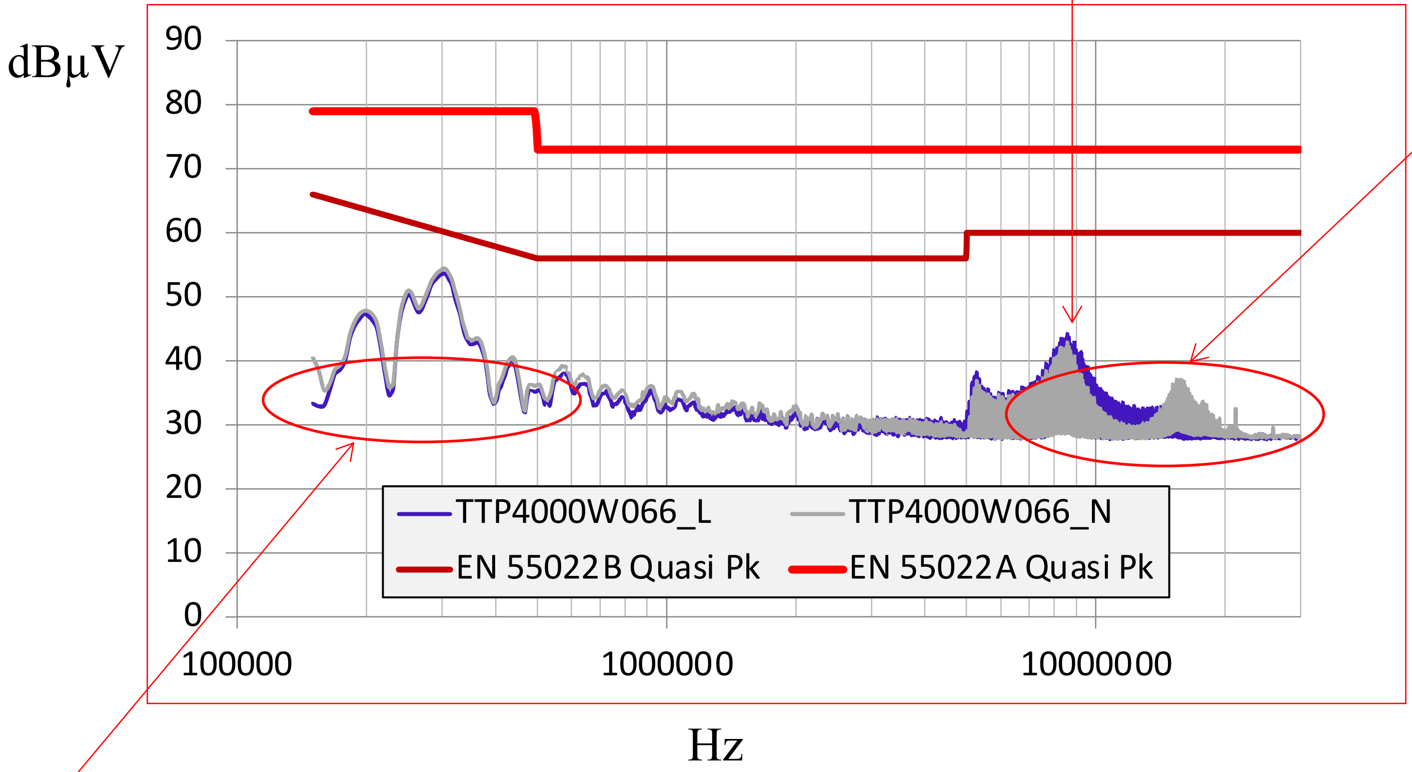
EMI Test

MICROCHIP

Add small loose inductor L6 to reduce the PFC inductor self-resonance noise peak.

Add 15 Ω Rg to slow down the switching speed to reduce high frequency noise.

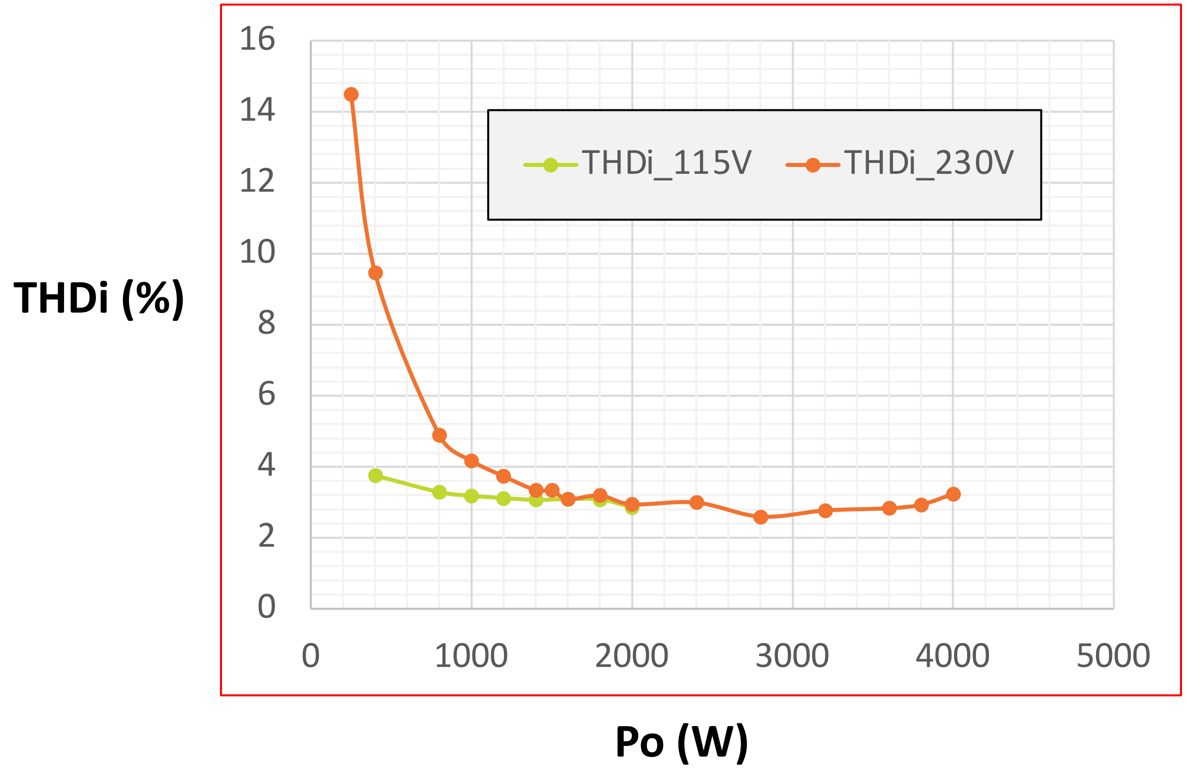


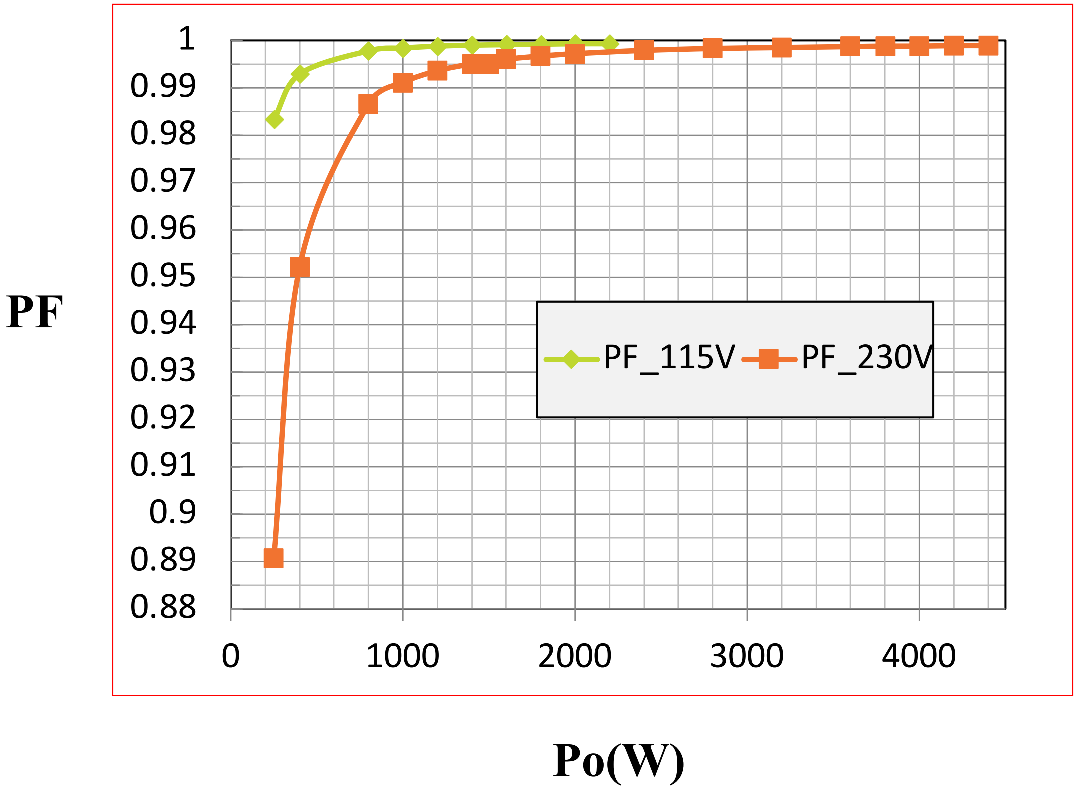
Use high permeability nano crystalline core to replace ferrite CM choke for lower copper loss and higher Lcm.

Meet EN 55022 Class A

Test conditions: Vin= 115V, Vo=385V, Po= 1050W

THDi and Power Factor





THDi_115V < 5%;
THDi_230V < 5% (@>25% Load)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Thank you!
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Highest Performance, Highest Reliability GaN