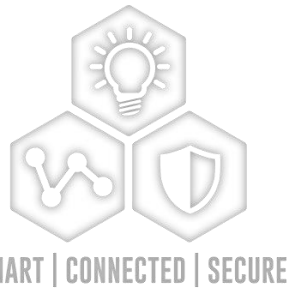
# Smart Embedded Vision with PolarFire and PolarFire SoC FPGAs


A Leading Provider of Smart, Connected and Secure Embedded Control Solutions




**Allen Chang**

Sep 2022

# Sections

- Microchip FPGA Strategy for Differentiation
- PolarFire® FPGAs
- PolarFire ® SoC FPGAs
- Smart Embedded Vision (SEV)
- SEV Success Stories
- Key SEV IP Details
- VectorBlox™ Accelerator

# Microchip FPGA Vision & Strategies

## Vision:

**To enable innovation by offering the**

**most power-efficient programmable solutions**

### Summary of Strategies:

- Focus on mid-range targeted applications
- Optimize architectures to maintain clear differentiators
  - 30%-50% lower total power
  - Highest security
  - Highest reliability
- Expand customer base in broad market sell
- Shift focus to solution-based platforms with increased software capability

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# FPGA Market TAM

- FPGA TAM 7% CAGR '27 to >$10B.

**2019-2021 PLD Sales Leaders ($M)**

| 2021 Rank | Company | 2019 ($M) | 19/18 % Change | 2019 Share | 2020 ($M) | % Change | 2020 Share | 2021 ($M) | % Change |
|---|---|---|---|---|---|---|---|---|---|
| 1 | Xilinx | 3,235 | 13% | 53% | 3,053 | -6% | 53% | 3,676 | 20% |
| 2 | Intel | 1,987 | -6% | 33% | 1,853 | -7% | 32% | 1,934 | 4% |
| 3 | Microchip | 376 | 16% | 6% | 387 | 3% | 7% | 436 | 13% |
| 4 | Lattice | 345 | -1% | 6% | 345 | 0% | 6% | 421 | 22% |
| 5 | Achronix | 100 | 3% | 2% | 105 | 5% | 2% | 115 | 10% |

Source: IC Insights, company reports

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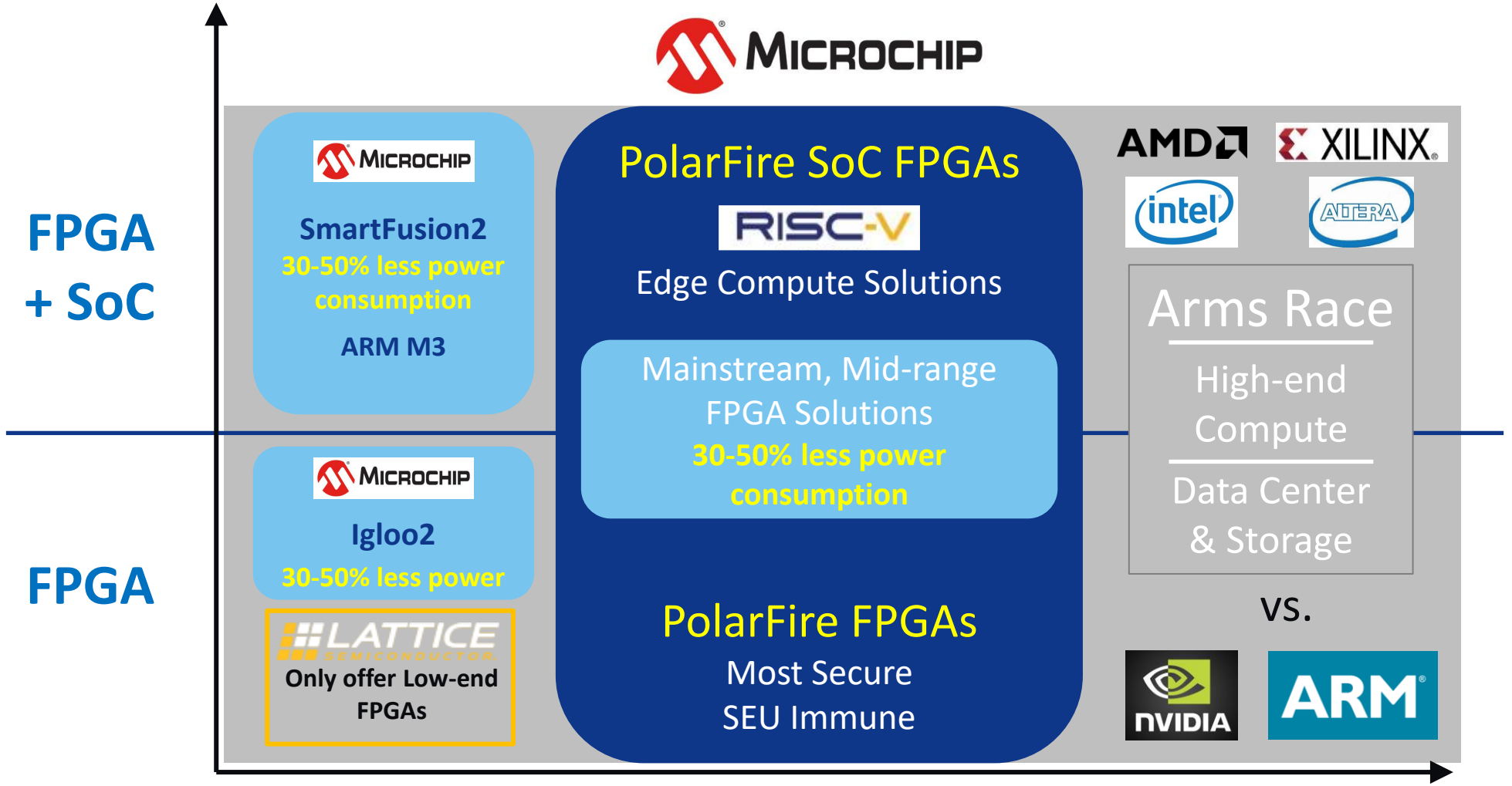
# Microchip FPGAs - It's all about FOCUS

## Lowest Power, Mid-Range FPGAs and SoC FPGAs




KLE = thousands of Logic Elements

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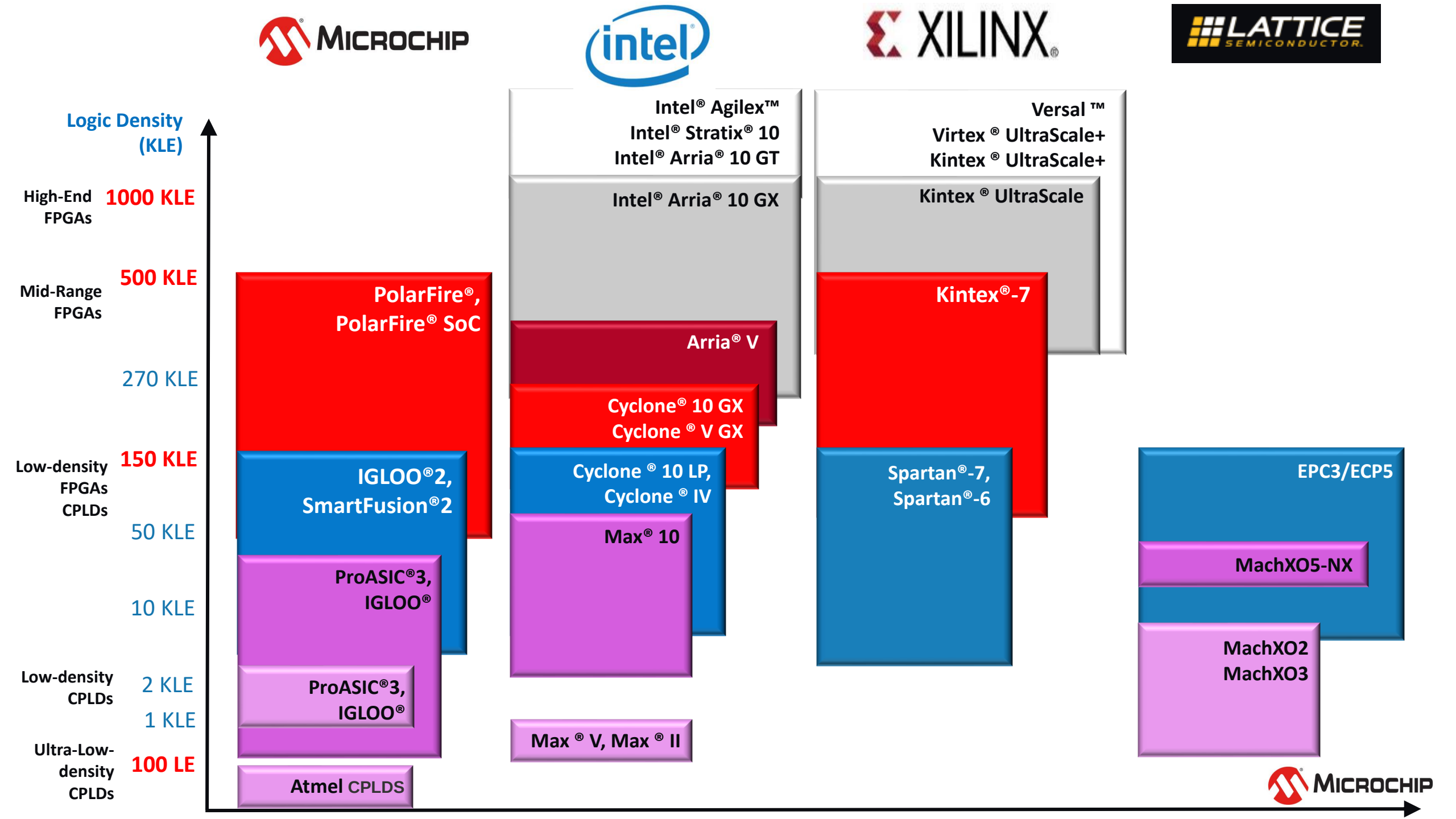
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intel
XILINX
LATTICE SEMICONDUCTOR
Logic Density (KLE)
High-End FPGAs
1000 KLE
Mid-Range FPGAs
500 KLE
270 KLE
Low-density FPGAs CPLDs
150 KLE
50 KLE
10 KLE
Low-density CPLDs
2 KLE
1 KLE
Ultra-Low-density CPLDs
100 LE
Intel® Agilex™
Intel® Stratix® 10
Intel® Arria® 10 GT
Intel® Arria® 10 GX
Versal ™
Virtex ® UltraScale+
Kintex ® UltraScale+
Kintex ® UltraScale
PolarFire®, PolarFire® SoC
Arria® V
Cyclone® 10 GX
Cyclone ® V GX
Kintex®-7
IGLOO®2, SmartFusion®2
Cyclone ® 10 LP, Cyclone ® IV
Spartan®-7, Spartan®-6
EPC3/ECP5
Max® 10
MachXO5-NX
ProASIC®3, IGLOO®
MachXO2
MachXO3
ProASIC®3, IGLOO®
Max ® V, Max ® II
Atmel CPLDS
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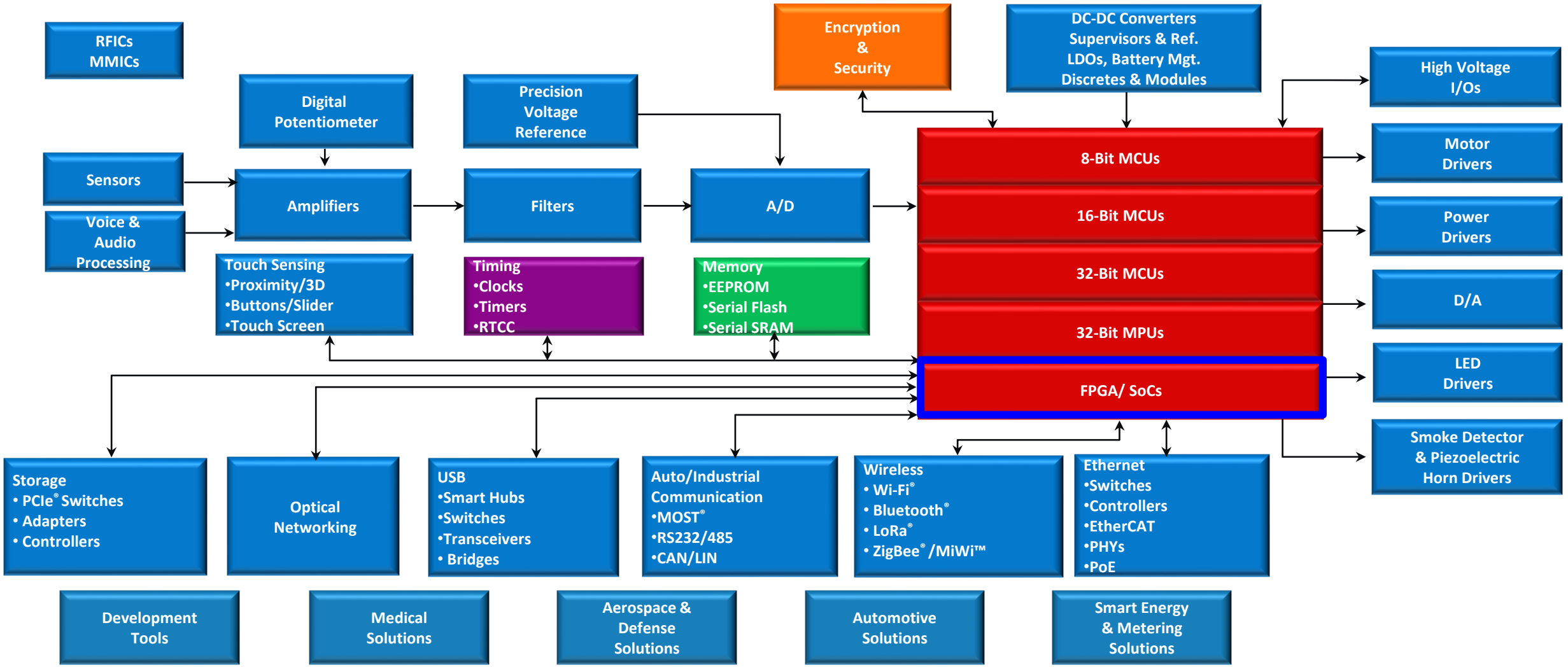
# Total System Solutions




~$400M per year FPGA Business Unit.

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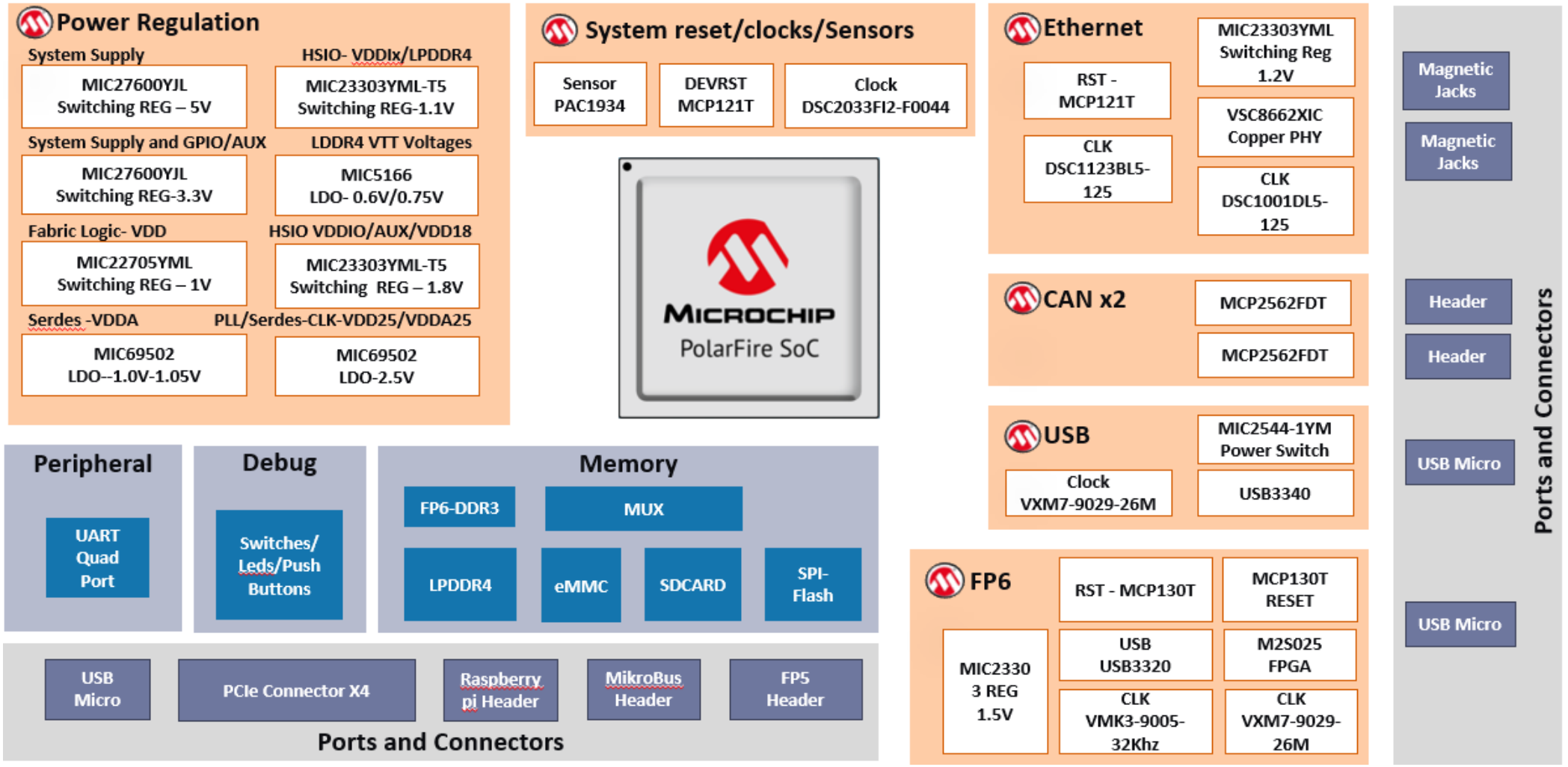
# Leader in Total Systems Solutions

## Simplify your design with Microchip optimized solutions

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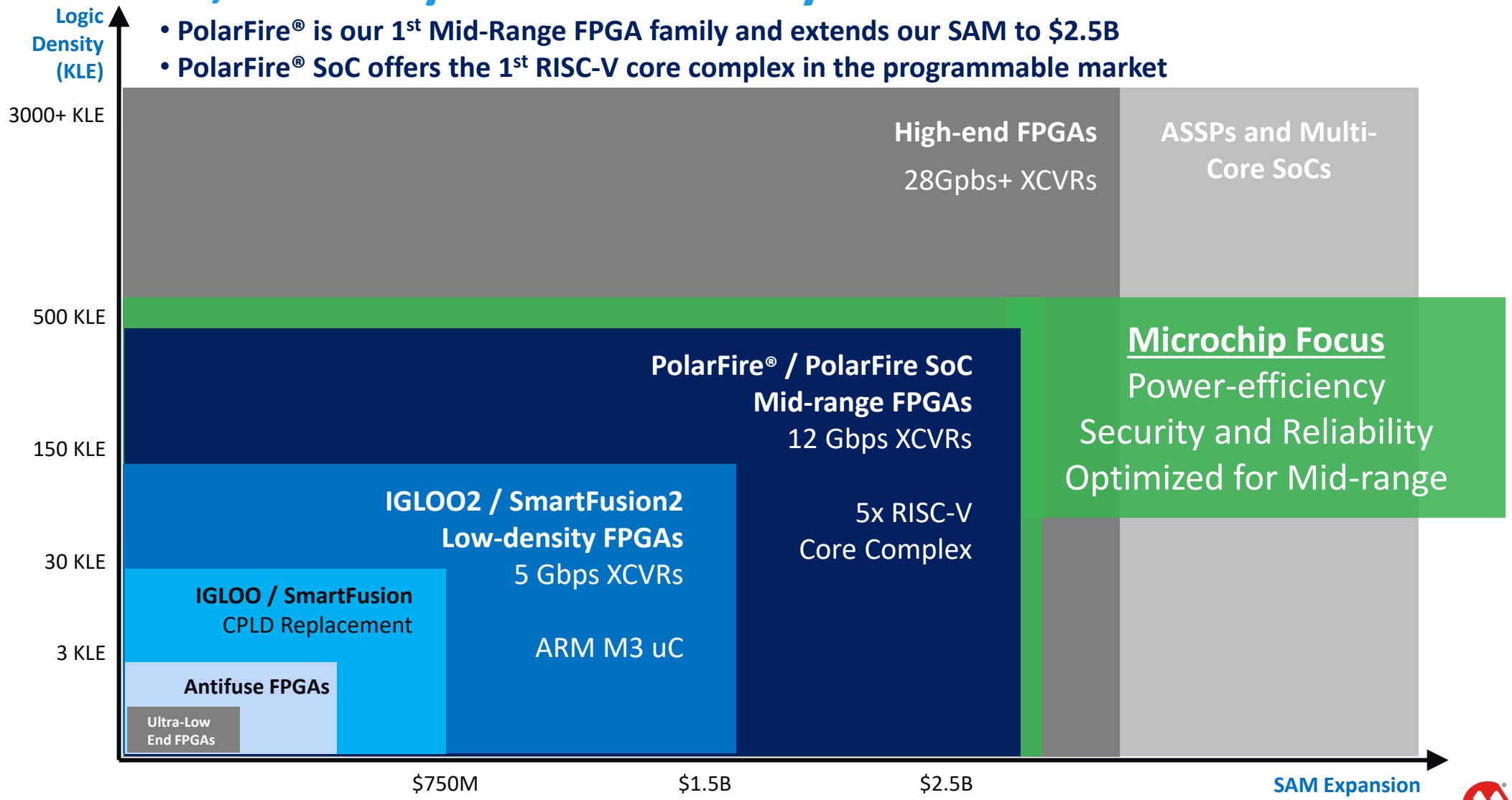
# Microchip FPGA / SoC Focus

## Low Power, Security and Reliability

- PolarFire® is our 1st Mid-Range FPGA family and extends our SAM to $2.5B
- PolarFire® SoC offers the 1st RISC-V core complex in the programmable market



# Significantly Lower Power Consumption

## By Technology and By Design

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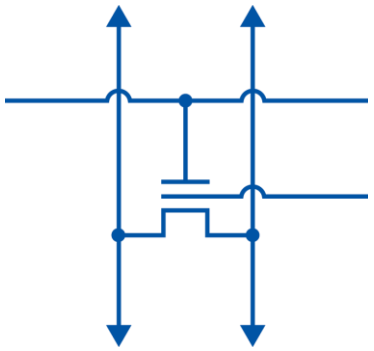
### Non-Volatile Cell



**Non-Volatile memory:** retains its state

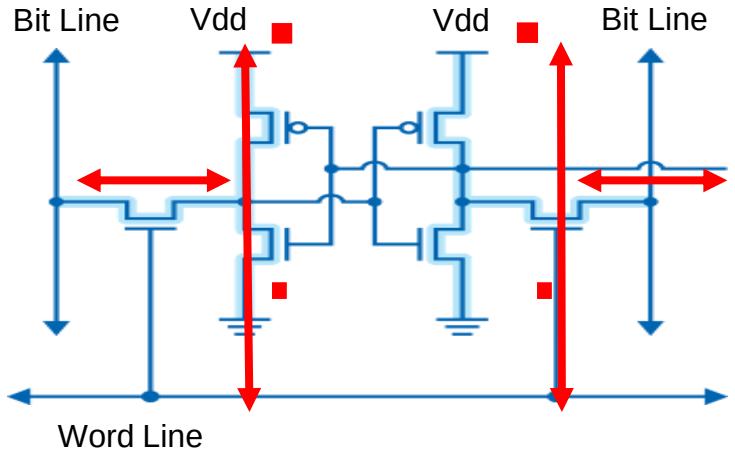
1000x lower leakage per cell

**Features:** designed for LOW POWER

(Transceivers, Microprocessors, etc)

XILINX intel

### SRAM Cell




**SRAM:** must continually re-charge

Substantial leakage per cell

**Features:** designed for HIGH-END market

(and re-used for mid-range families)

**Total Power Savings of 30-50% vs SRAM FPGAs**

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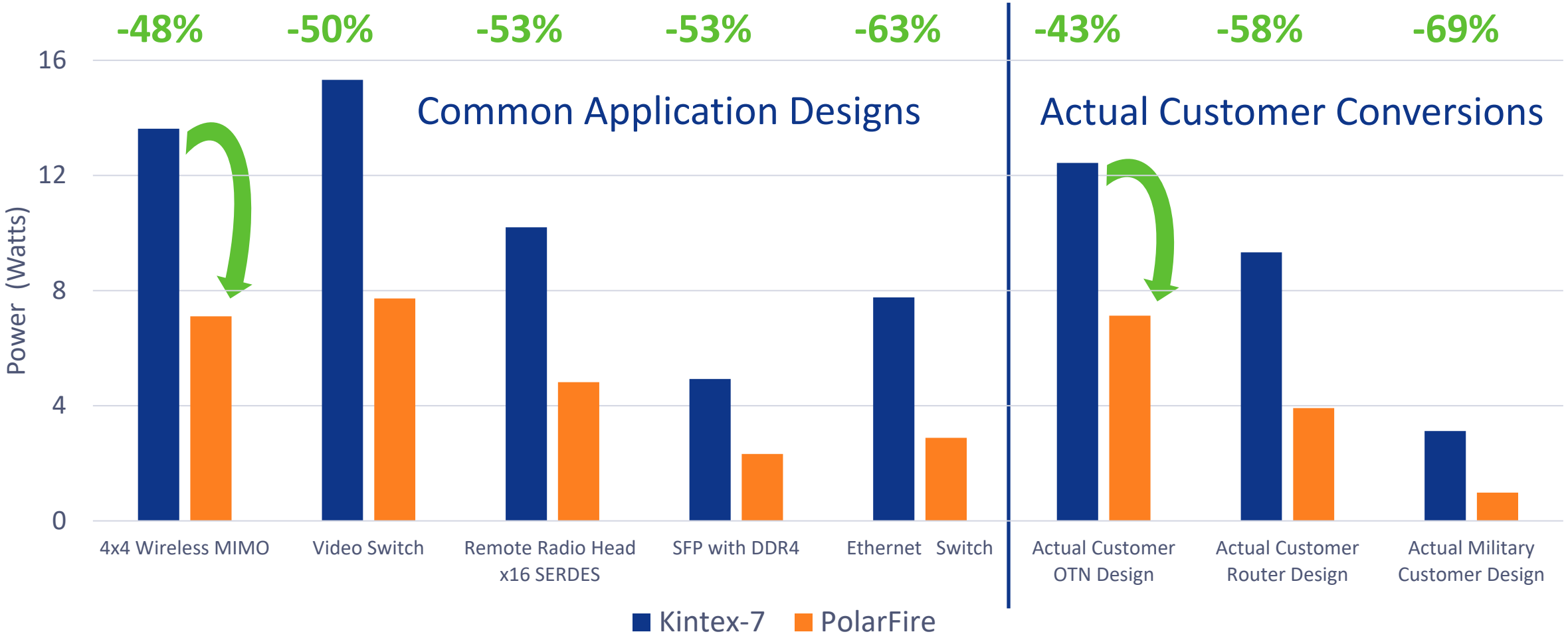
# PolarFire Power Savings by Design

## Lowest Power – saving 43% to 69% versus Kintex-7 from Xilinx




All designs using official Xilinx and Microchip layout and power estimation tools with common effort levels
All designs using PolarFire standard speed devices versus Kintex-7 -2LI devices (Kintex-7's low-power-binned devices; similar performance devices)

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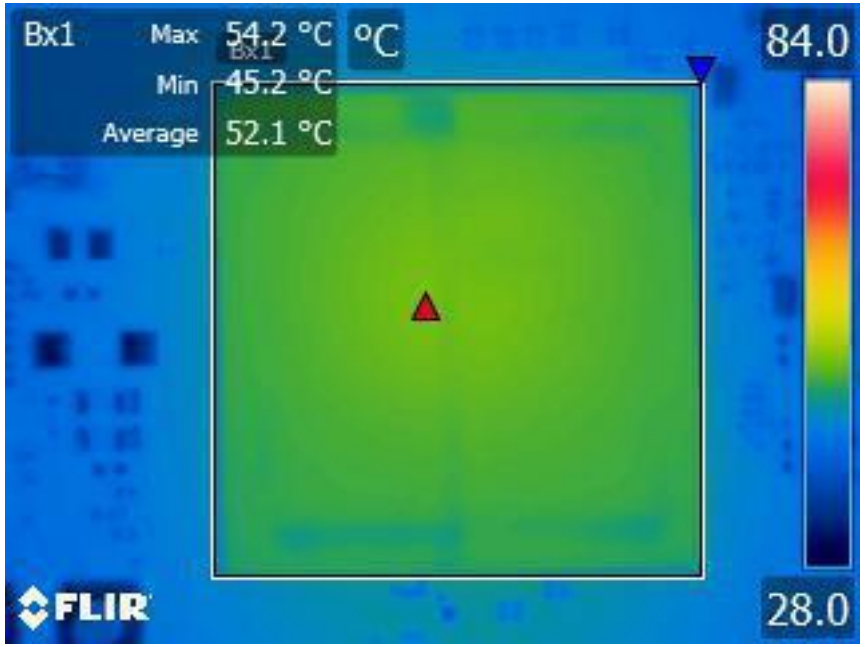
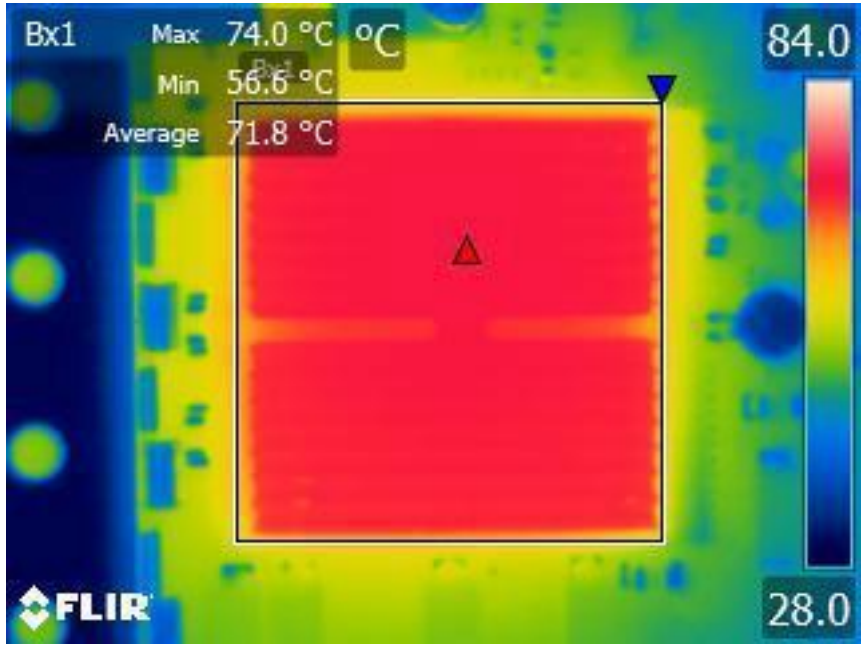
# Thermal Comparison - $1.5 / W to Dissipate Heat

## Four 5 Gbps Xcvrs, 800 160 MHz RAM Blocks, Logic, and 6 PLLs




PolarFire FPGA
2.7W




Kintex-7 FPGA
5.5W



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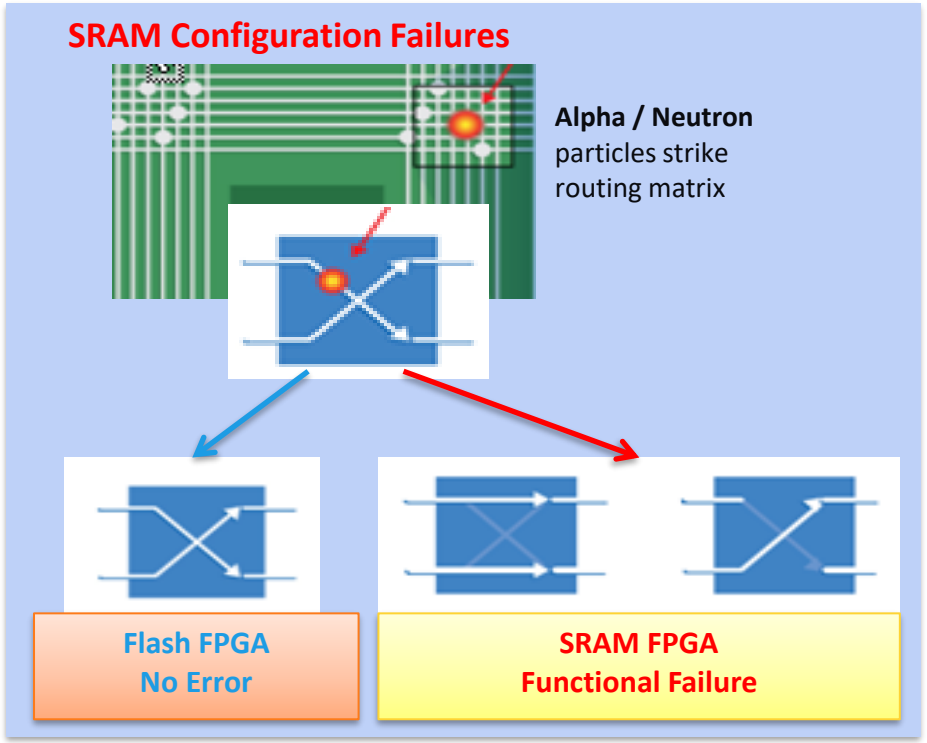
# Exceptional Reliability

- **Error Free SEU immune Fabric Configuration**
  - No need to detect configuration errors
    - No scrubbing required
    - No triple mode redundancy needed
    - Lowers cost
- **Block RAM with ECC**
  - Built-in SECDED on 33-bit word
- **System Controller Suspend Mode for Safety Critical Applications**




*SEU Immune fabric simplifies your design & increases reliability*

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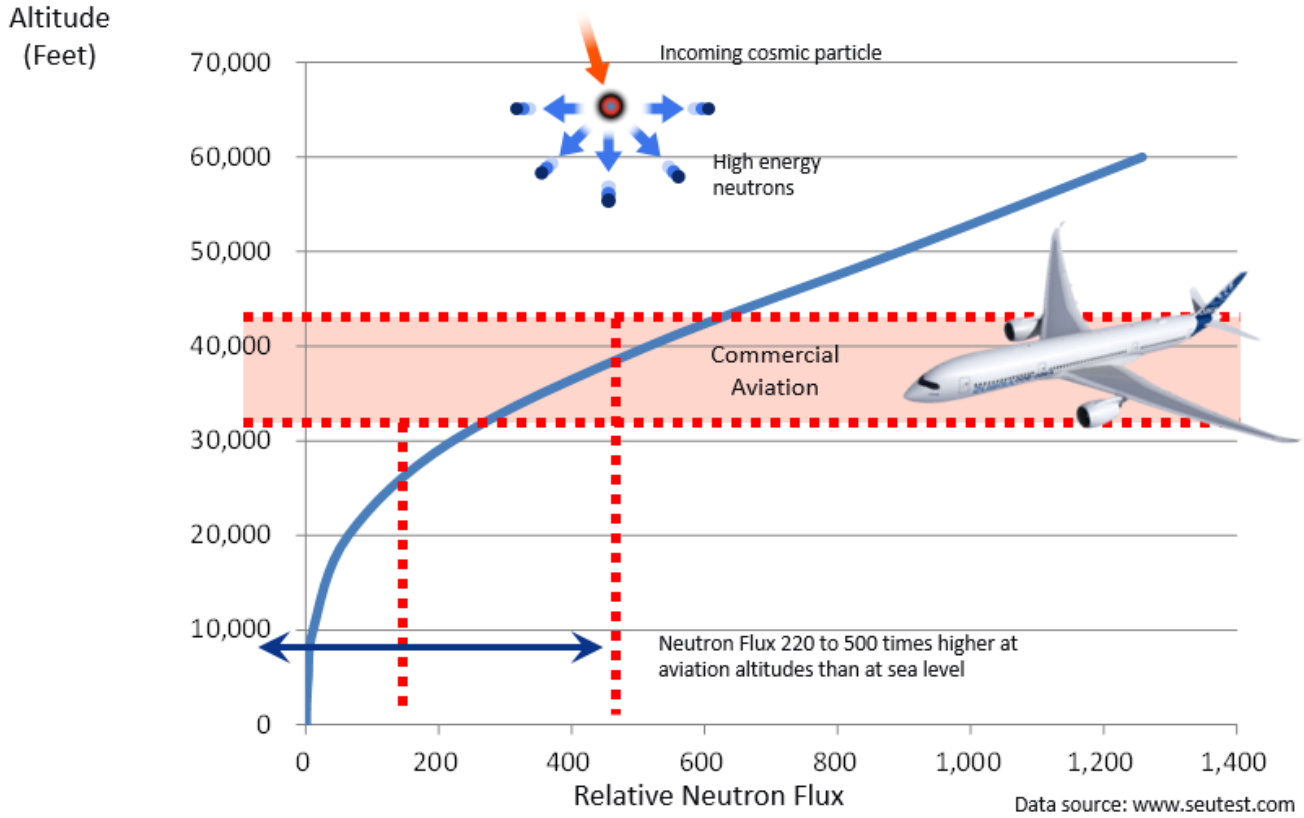
# Radiation Effects in Electronics

- **Electronic devices experience neutron effects up to 500 times more frequently at commercial aviation altitudes than at sea level**
- **500 pieces of electronic equipment at sea level = 1 piece of electronic equipment on an airplane**




14 Neutrons/ $CM^2$/hour at sea level

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# High Reliability Screening and Qualification

- **Supported qualification standards**
  - JEDEC
  - JEDEC+
    - ELFR 48hr Burn-In
      - $V_{DD}$+20% & Tj (140C) vs Datasheet specs
  - AECQ-100
  - Mil Std 883 Class B
  - PEMs qual on request
- **Gold bond wire options**

| Commercial | Industrial | Automotive T2/T1 | Mil Temp | Mil-Std 883 class B |
|---|---|---|---|---|
| Wafer Sort | Wafer Sort | Wafer Sort | Wafer Sort | Wafer Sort |
| Package Assembly | Package Assembly | Package Assembly | Package Assembly | Package Assembly |
| Final Test +25°C | Final Test +25°C | Burn-in (Dyn, Opt.) | Final Test +25°C | Internal Visual |
| | Sample Test +100°C | Final Test +25°C | Final Test -55°C | Temp. Cycling |
| | | Final Test +125/135°C | Final Test +125°C | Const. Acceleration |
| | | | | PIND |
| | | | | Visual |
| | | | | Electrical Test |
| | | | | Dynamic Burn-in |
| | | | | Final Test +25°C |
| | | | | Final Test -55°C |
| | | | | Final Test +125°C |
| | | | | Seal |
| | | | | Group A Lot Sample |
| | | | | Group B Lot Sample |
| QC Mon. Sample | QC Mon. Sample | QC Mon. Sample | QC Mon. Sample | QC Mon. Sample |

# Dependable Longevity of Supply

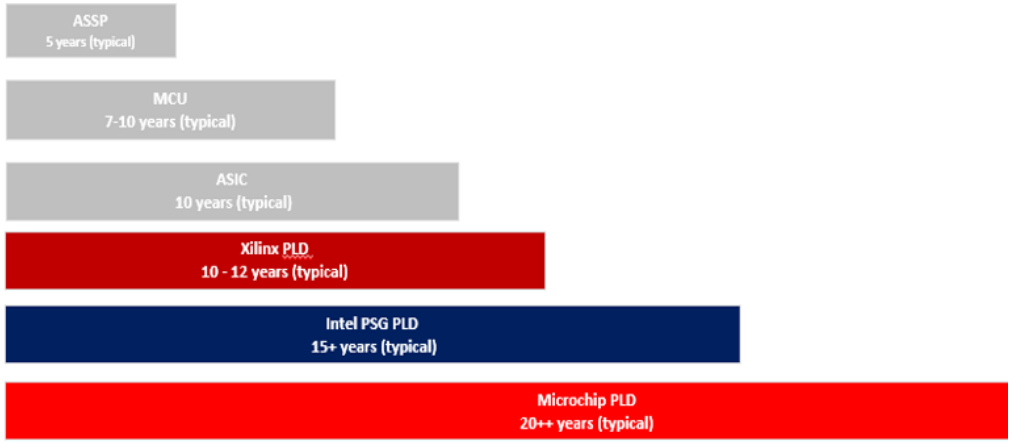
February 2, 2021

Dear Valued Customer,

Thank you for your continued interest in Microchip/Microsemi FPGA products. The purpose of this letter is to address Microchip/Microsemi's FPGA product longevity. Below you will find a matrix of device families with data on when parts first shipped and an approximate timeframe that we expect to have wafer availability; please note that this is not a guarantee of availability.

| Device Family Name | Microsemi Part Number Starts With… | Year First Shipped | Expected Availability from 2021 |
|---|---|---|---|
| MX | A40MX, A42MX | 1997 | 10 years |
| SX | A54SX | 1999 | 5 years |
| SXA | A54SX_A | 1999 | 10 years |
| AX | AX | 2001 | 10 years |
| eX | eX | 2001 | 10 years |
| ProAsic Plus | APA | 2001 | 10 years |
| ProAsic 3 | A3P, A3PN, A3PL | 2005 | 10 years |
| Igloo | AGL, AGLN | 2005 | 10 years |
| Igloo Plus | AGLP | 2005 | 10 years |
| Fusion | AFS | 2006 | 10 years |
| SmartFusion | A2F | 2010 | 10 years |
| SmartFusion 2 | M2S | 2013 | 15 years |
| Igloo 2 | M2GL | 2013 | 15 years |
| PolarFire | MPF | 2017 | 20 years |

**Product Life Cycle:**



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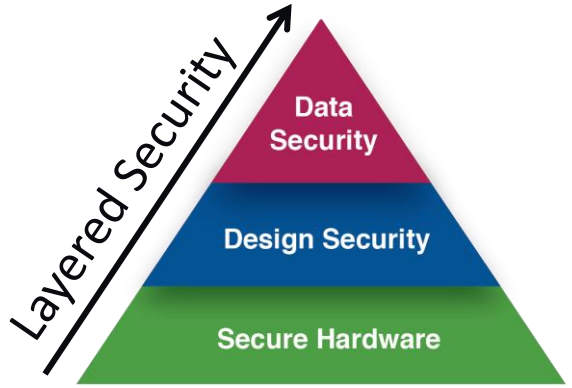
# Industry's Best FPGA Security

**Cyber Security is the #1 concern for connected devices on the network edge**

$400 of DPA hacking equipment can lead to millions of dollars in IP theft

| Security Advantage | Low Density | | Mid-Range | |
|---|---|---|---|---|
| | Microchip | Competition | Microchip | Competition |
| Prevent Overbuilding and Cloning | Best Low Density Security | N/A | Best Security In The Industry | N/A |
| Full Design IP Protection | | N/A | | Weak |
| Root of Trust | | N/A | | Weak |
| Secure Data Communications | | N/A | | Weak |
| Anti-Tamper | | N/A | | N/A |



# FPGA Market - 1

- **Based on Configuration:**
  - Low-End FPGA
  - Mid-Range FPGA
  - High-End FPGA
- **Based on node size:**
  - ≤16 NM
  - 22/28-90 NM
  - >90 NM
- **Based on technology:**
  - SRAM
  - Flash
  - Antifuse

# FPGA Market - 2

- **Based on vertical:**
  - Data Centers & Computing
  - Telecommunications
  - Consumer Electronics
  - Test, Measurement & Emulation
  - Military & Aerospace
  - Industrial
  - Automotive
  - Healthcare
  - Multimedia
  - Broadcasting

# FPGA Market - 3

- **Industrial**
  - Video Surveillance Systems
  - Machine Vision Solutions
  - Industrial Networking Solutions
  - Industrial Motor Control Solutions
  - Robotics
  - Industrial Sensors
- **Automotive**
  - ADAS
  - Automotive Infotainment and Driver Information Systems
  - Sensor Fusion
- **Healthcare**
  - Imaging Diagnostic Systems
    - Ultrasound Machines
    - Endoscope
    - CT Scanners
    - X-Ray Machines
  - Wearable Devices
- **Multimedia**
  - Audio Devices
  - Video Processing
- **Broadcasting**
  - Broadcast Platform Systems
  - High-End Broadcast Systems

# Introduction to PolarFire FPGA Family

Cost Optimized, Mid-Range density FPGAs

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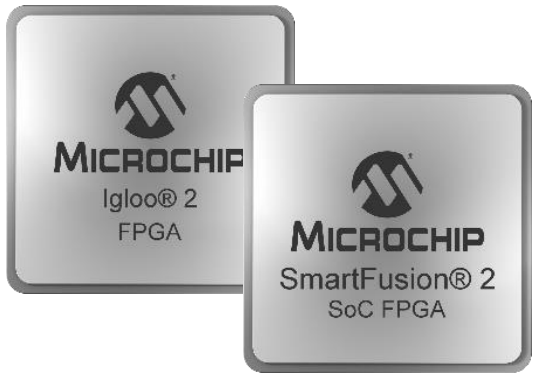
# Broad Range FPGA Supplier


***Smallest Packages***
***CPLD Replacements***




***More Resources***
***Low Density FPGAs***


***Cost Optimized***
***Mid-Range Density FPGAs***


***Quad Core RISC-V***
***Real-time Linux***

**Up to 50% Lower Power**

**Proven Security**

**SEU Immune FPGA Configuration**

**Instant-on and Non-volatile**

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# PolarFire FPGAs

## PolarFire Cost-optimized FPGAs Deliver the Lowest Power at Mid-range Densities

- **Cost Optimized**
  - Architecture and process optimizations Mid-Range densities
  - Smallest area high-speed I/Os
  - Area optimized 12.7G transceivers
  - 1.6 Gbps LVDS I/Os supporting DDR4/DDR3/LPDDR3
  - Plus hardened I/O gearing logic with CDR (supports SGMII/GbE on GPIOs)
  - Lower BOM costs
    - 0°C-100°C at commercial temp prices
- **Lowest Power**
  - Lowest static power
  - Up to 50% lower power than competing FPGAs
- **Proven Security with Exceptional Reliability**



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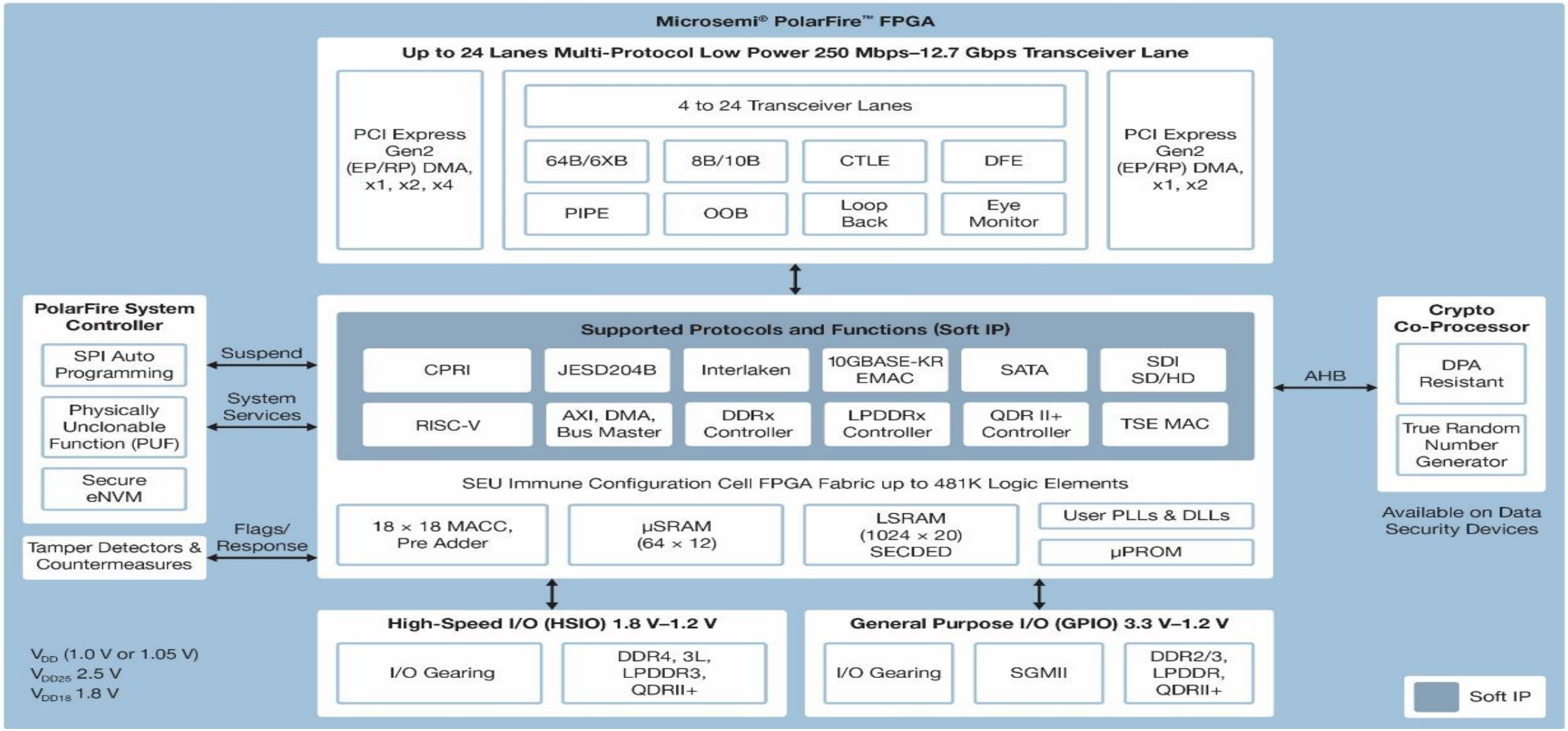
# PolarFire FPGA Architecture




*PolarFire FPGAs cost-optimized, lowest power at mid-range densities*

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# Lowest Power – Up to 50% Lower than Competitors

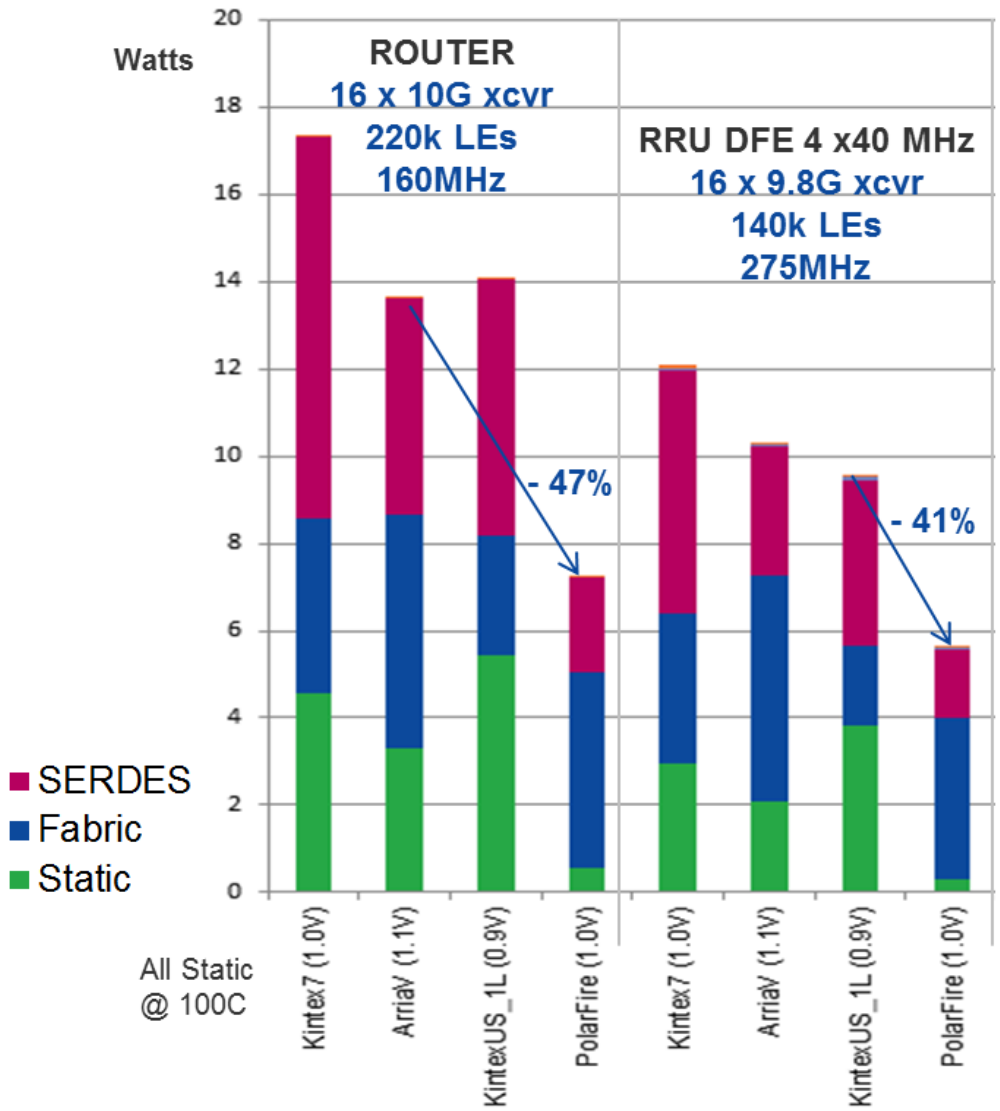
- **Enabling Application Performance at Significantly Lower Power**

Static power: 10x Reduction

Transceiver power: 2x Reduction

***Total power up to 50% lower than best case competitor number***

***PolarFire Customer: "$1.5/W in BOM cost saving due to power savings"***

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# Smallest Form Factors

## Best-in-Class at 100K, 200K & 300K LEs

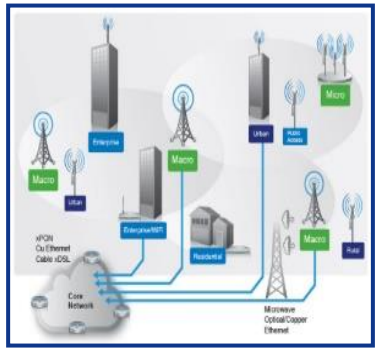

**MPF100**
**11x11 mm**


**MPF200**
**11x14 mm**


**MPF300**
**16x16 mm**

# PolarFire FPGAs

## Best in Class Capabilities



**Communications**
- Wireline Access
- Wireless HetNet
- Wireless Backhaul
- Smart Optical Modules
- Video Broadcasting

**Defense and Aviation**
- Secure Embedded Systems
- Secure Communications
- Intelligence and Surveillance,
- Guidance, Radar & Electronic Warfare
- Aircraft Data Networking, Actuation, Avionics

**Industrial**
- Process Control & Automation
- Industrial Image Processing & Analytics
- Programmable Logic Controllers
- Industrial Networking

**Best In Class Capabilities**
- Lowest Power
- Lowest Cost 10G SERDES Based FPGA
- Lowest Cost DDR4 and High-speed I/O Solutions
- Smallest Form Factors
  11x11mm 100KLE
  11x14.5mm 200KLE
  16x16mm 300KLE
- Highest Security
- SEU Immune fabric
- Non-volatile, no configuration chip required
- 2-5x More 3.3V I/O

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# PolarFire Product Family

| | Features | MPF050 | MPF100 | MPF200 | MPF300 | MPF500 |
|---|---|---|---|---|---|---|
| FPGA Fabric | Logic Elements (4LUT + DFF) | 48K | 109K | 192K | 300K | 481K |
| | Math Blocks (18x18 MACC) | 150 | 336 | 588 | 924 | 1480 |
| | LSRAM Blocks (20 kbit) | 160 | 352 | 616 | 952 | 1520 |
| | uSRAM Blocks (64x12) | 450 | 1008 | 1764 | 2772 | 4440 |
| | Total RAM (Mbits) | 3.6 Mbits | 7.6 Mbits | 13.3 Mbits | 20.6 Mbits | 33 Mbits |
| | uPROM (kbits | 216 Kbits | 297 Kbits | 297 Kbits | 459 Kbits | 513 Kbits |
| | User DLL's/PLL's | 8 each | 8 each | 8 each | 8 each | 8 each |
| High Speed I/O | 250 Mbps -12.7 Gbps Transceiver Lanes | 4 | 8 | 16 | 16 | 24 |
| | PCIe Gen2 Endpoints/Root Ports | 2 | 2 | 2 | 2 | 2 |
| Total I/O | Total User I/O | 176 | 284 | 364 | 512 | 584 |
| Packaging | Type / Size / Pitch | | Total User I/O (HSIO / GPIO) GPIO CDRs / XCVRs | | | |
| | FCSG325 (11x11, 11x14.5*, 0.5 mm) | 164(84/80) 6/4* | 170(84/86) 8/4 | 170(84/86) 8/4 | | |
| | FCSG536 (16x16, 0.5 mm) | | | 300(120/180) 15/4 | 300(120/180) 15/4 | |
| | FCVG484 (19x19, 0.8 mm) | 176(96/92) 7/4* | 284(120/164) 14/4 | 284(120/164)14/4 | 284(120/164) 14/4 | |
| | FCG484 (23x23, 1.0 mm) | | 244(96/148) 13/8 | 244(96/148) 13/8 | 244(96/148) 13/8 | |
| | FCG784 (29x29, 1.0 mm) | | | 364(132/232) 20/16 | 388(156/232) 20/16 | 388(156/232) 20/16 |
| | FCG1152 (35x35, 1.0 mm) | | | | 512(276/236) 24/16 | 584(324/260) 24/24 |
| | | | Devices in the same package and family type are pin compatible | | | |

**Extended Commercial (0°C-100°C) and Industrial (-40°C-100°C) temperature support for all die package combinations**

***Automotive (-40°C-125°C) Junction Temperature***

***AEC-Q Qual Vehicle***

***Automotive qualified devices are available today***

**Devices go to production in 2022, AECQ-100 +6 months*

# Introduction to PolarFire SoC

Industry's 1st RISC V based SoC FPGA

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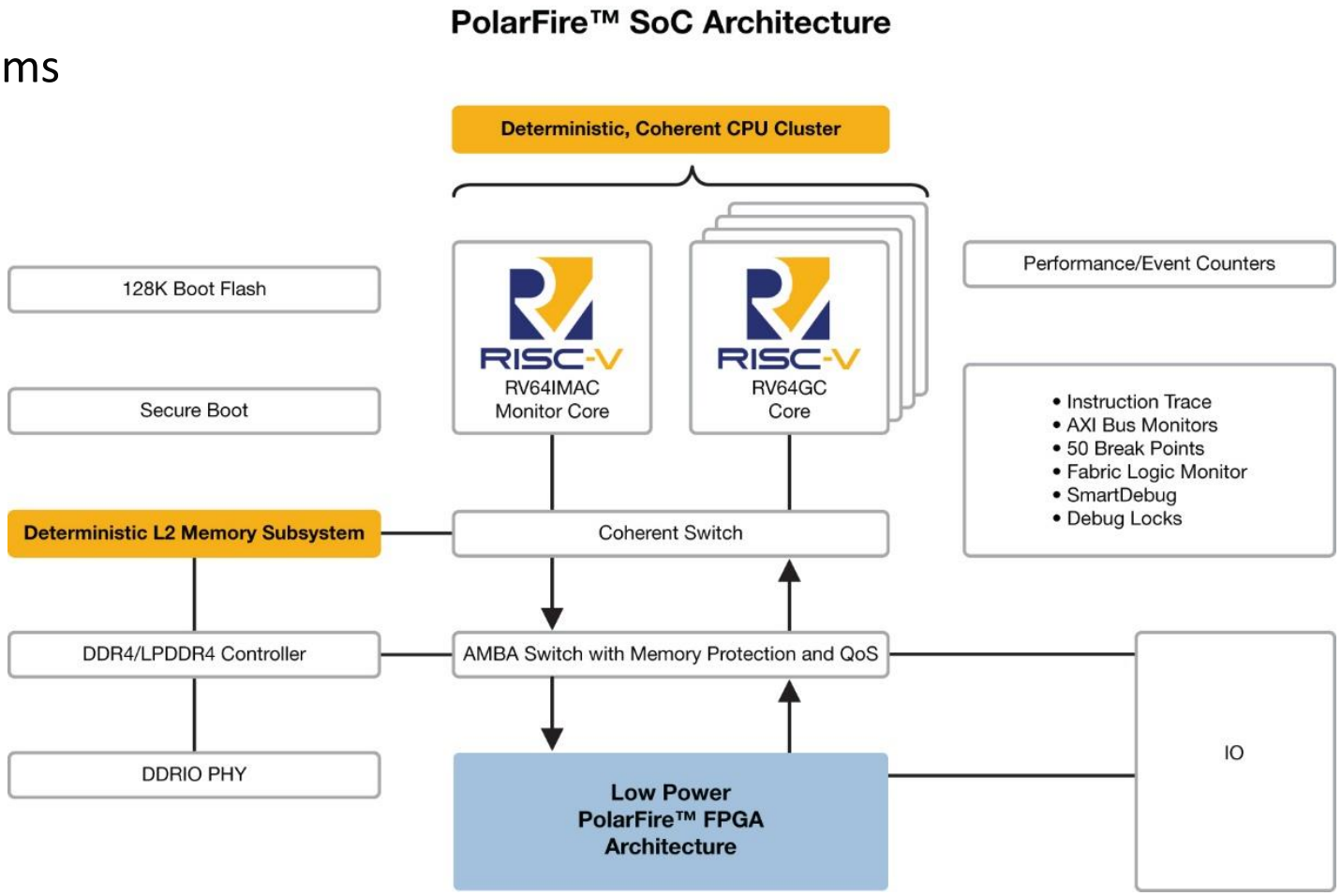
# PolarFire SoC enabled innovation platform

- **Freedom to innovate in**
  - Linux and Real-Time
  - Thermal and Power Constrained Systems
  - Securely Connected IoT Systems
  - High-Rel Safety Critical Systems

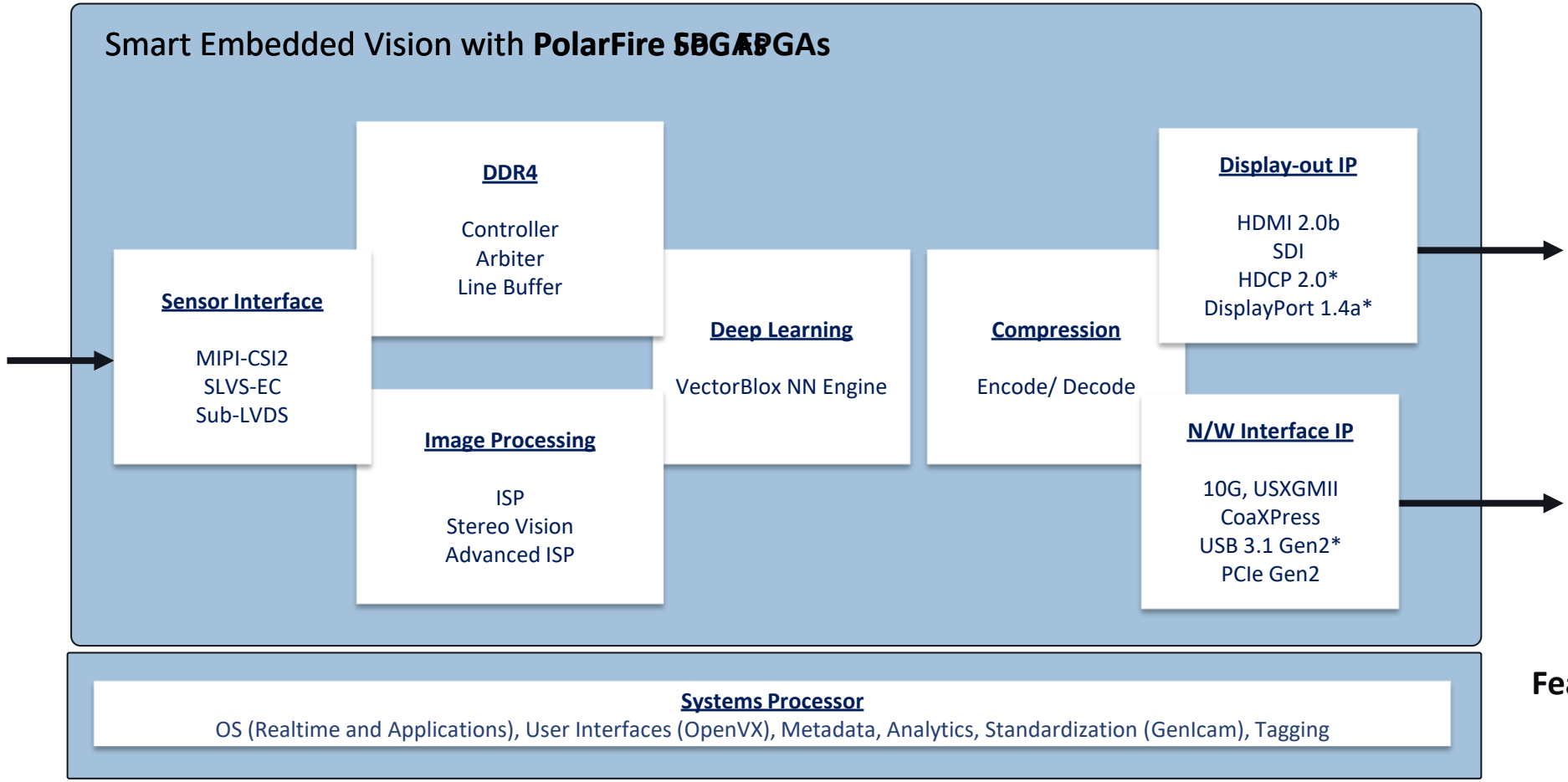



SiFive

ultraSoC

Microchip

# PolarFire SoC in Smart Embedded Vision




**Features enabled by PolarFire SoC**

**PolarFire SoC extends usability to a single-chip Vision and AI Solution**

* Third Party

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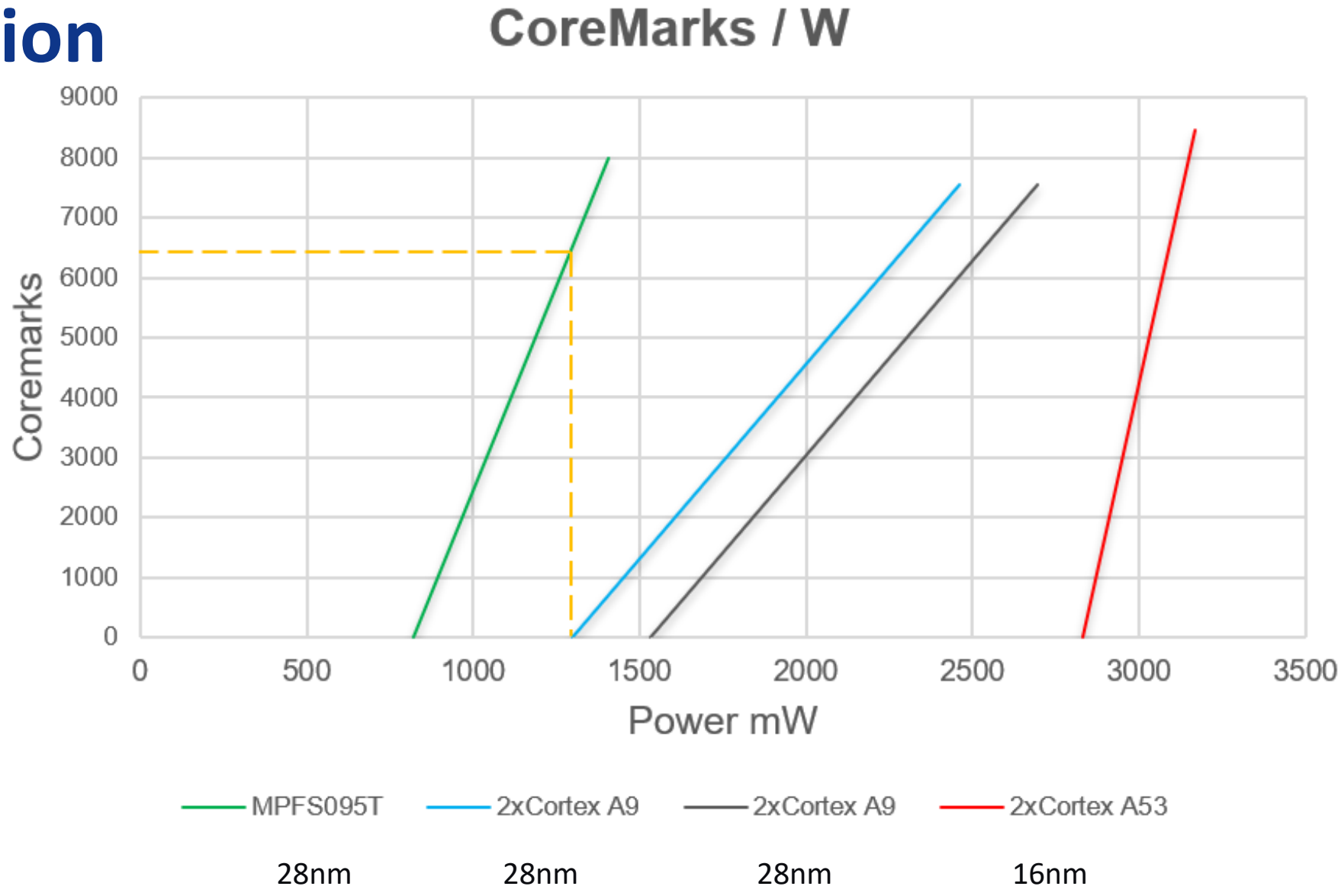
# PolarFire® SoC FPGA – Most Power Efficient SoC Solution

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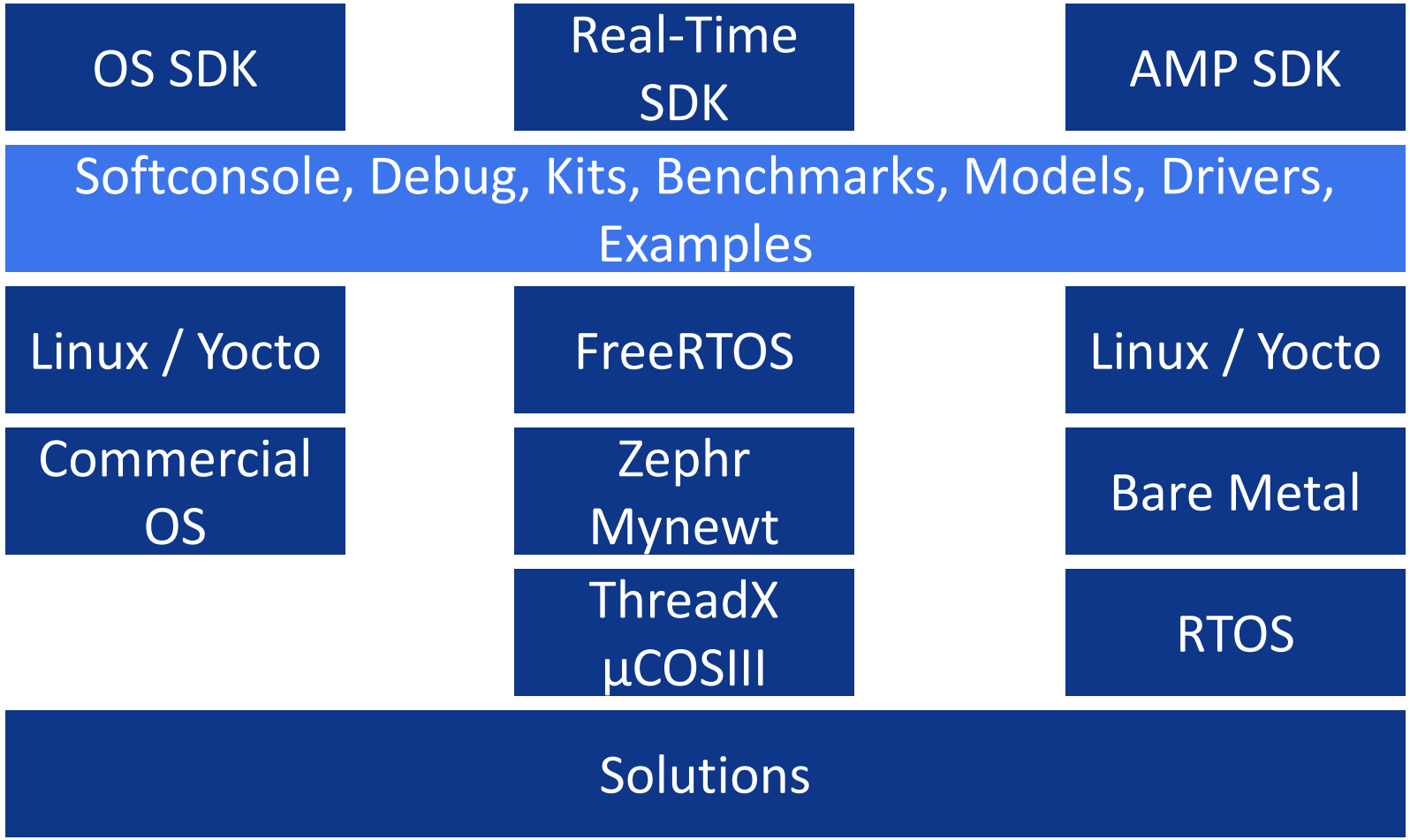
# Software Development Kits (SDK)




***Common PolarFire SoC use models supported with software development kits***

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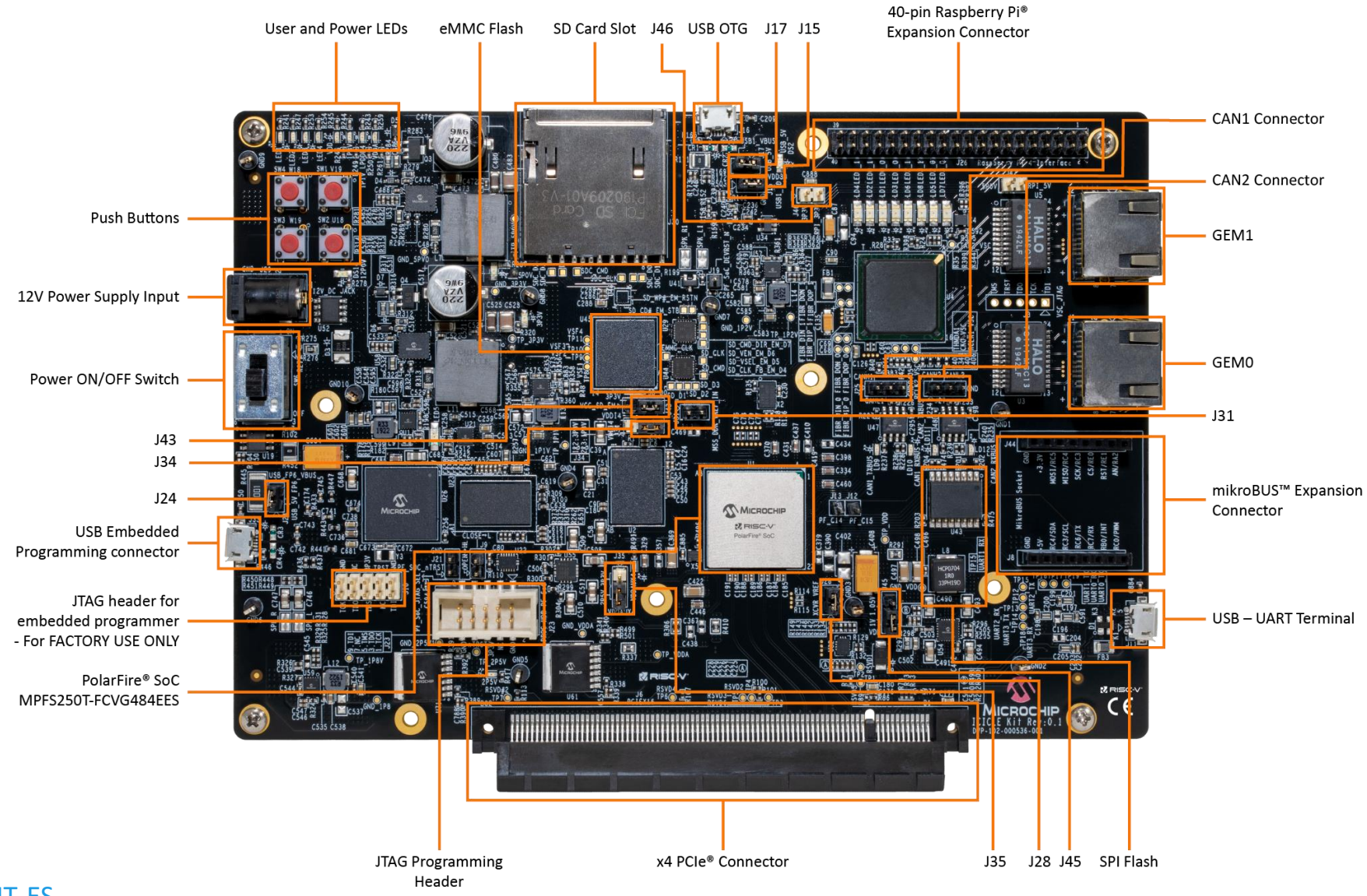
# PolarFire SoC Rollout

| | Features | MPFS025T | MPFS095T | MPFS160T | MPFS250T | MPFS460T |
|---|---|---|---|---|---|---|
| FPGA Fabric | K Logic Elements (4LUT + DFF) | 23 | 93 | 161 | 254 | 461 |
| | Math Blocks (18x18 MACC) | 68 | 292 | 498 | 784 | 1420 |
| | LSRAM Blocks (20k bit) | 84 | 308 | 520 | 812 | 1460 |
| | uSRAM Blocks (64x12) | 204 | 876 | 1494 | 2352 | 4260 |
| | Total RAM Mbits | 1.8 | 6.7 | 11.3 | 17.6 | 31.6 |
| | uPROM Kbits | 194 | 387 | 415 | 470 | 553 |
| | User DLL's/PLL's | 8 each | 8 each | 8 each | 8 each | 8 each |
| High Speed IO | 250 Mbps to 12.5 Gbps SERDES Lanes | 4 | 4 | 8 | 16 | 20 |
| | PCIe Gen2 End Points/Root Ports | 2 | 2 | 2 | 2 | 2 |
| Total FPGA IO | HSIO+GPIO | 108 | 276 | 312 | 372 | 468 |
| Total MSS IO | MSS IO | 136 | 136 | 136 | 136 | 136 |
| MSS DDR DB | MSS DDR Data Bus | 16 | 32 | 32 | 32 | 32 |
| Packaging | Type/Size/Pitch | Initial Production Dates | | | | |
| | FCSG325 (11x11, 0.5 mm) | Dec 2021 | CQ1 2022 | | | |
| | FCSG536 (16x16, 0.5 mm) | | CQ1 2022 | CQ2 2022 | Oct 2021 / Dec 2021 | |
| | FCVG484 (19x19, 0.8 mm) | Dec 2021 | CQ1 2022 | CQ2 2022 | Oct 2021 / Dec 2021 | |
| | FCVG784 (23x23, 0.8 mm) | | CQ1 2022 | CQ2 2022 | Oct 2021 / Dec 2021 | |
| | FCG1152 (35x35, 1.0 mm) | | | | Oct 2021 / Dec 2021 | CQ1 2022 / CQ3 2023 |

| | |
|---|---|
| Oct 2021 | Preproduction Parts in Industrial Grade with Schedule |
| Dec 2021 | Industrial Grade with Schedule |
| | Automotive T2 Grade (+1 year from the schedule shown) |

# PolarFire® SoC FPGA Icicle Kit




MPFS-ICICLE-KIT-ES
MSRP $562 – Available Now

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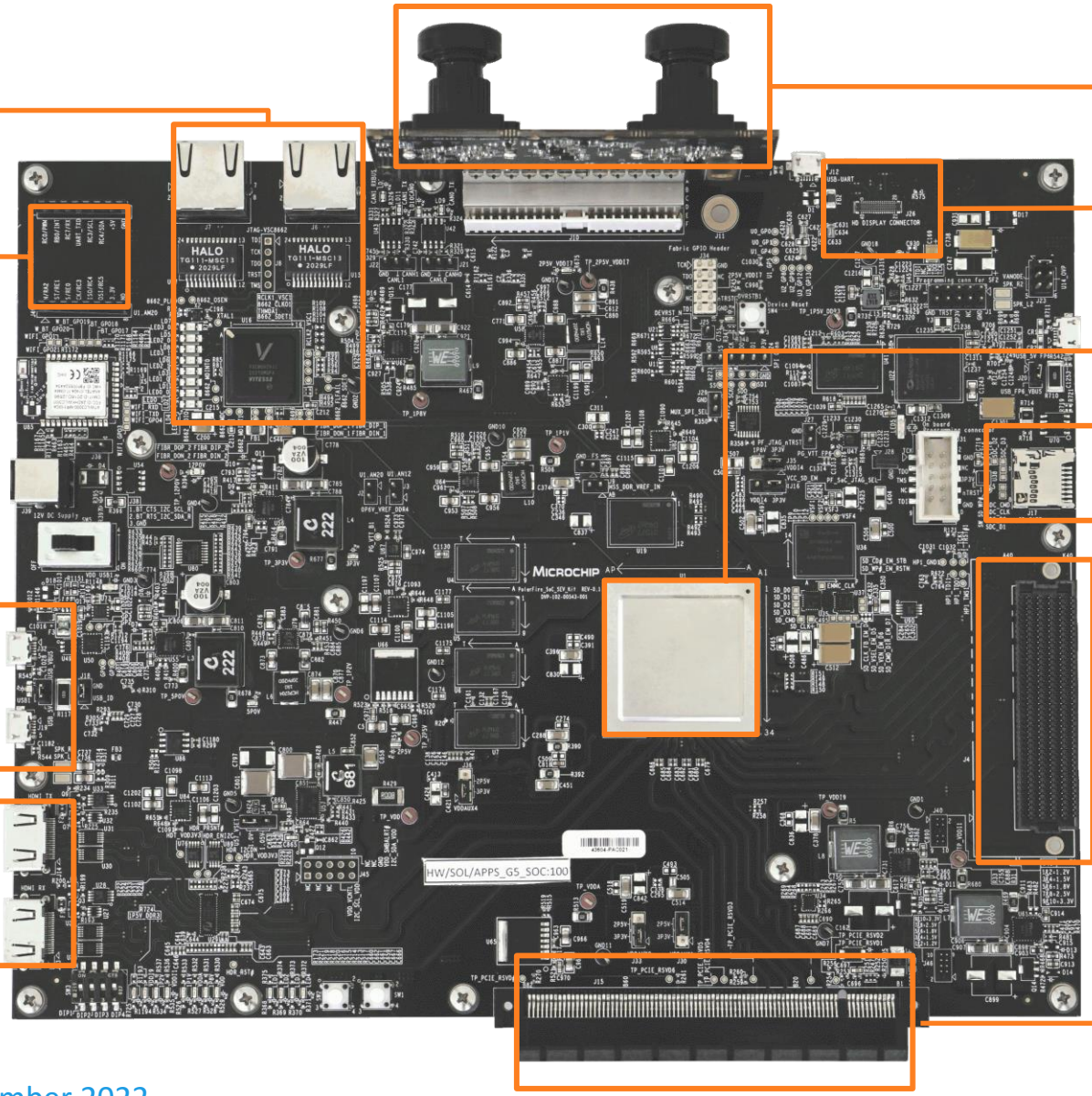
# The PolarFire® SoC FPGA Video Kit




MPFS250-VIDEO-KIT
MSRP $1839 – Shipping December 2022



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# Introduction to Smart Embedded Vision

Smart Embedded Vision with PolarFire FPGAs

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# PolarFire family of FPGAs and SoC FPGAs

## Driving your next generation Smart-Embedded-Vision Platform

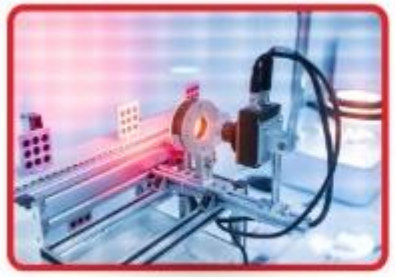

Virtual Reality


Drive Assist Systems


Drone Vision


Augmented Reality


Medical Vision


Machine Vision


Satellite Vision


Broadcast


Physical Security


Thermal Vision

- **Target next-gen embedded vision customer platforms**
- **Low power, small form factor and portable designs**
  - More thermal head room on the edge
  - Higher resolution – multiple 4K channels
  - Integrate Artificial Intelligence and Machine Learning
- **Alleviating customer concerns on Security and Reliability on the edge.**
- **VectorBlox™ Software Development Kit and Neural Network IP**

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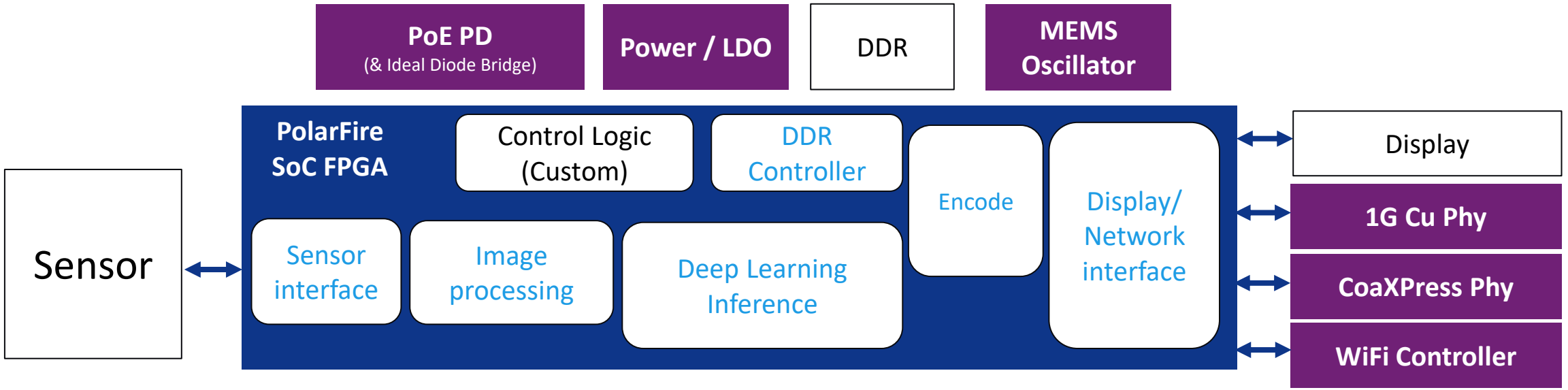
# SEV: A Microchip One-Stop-Shop




- **Sensor Interfaces (Rx)**
  - MIPI CSI-2 Receive (1.5 Gbps / lane)
  - SLVS-EC (4.7 Gbps / lane)
- **Display Interfaces**
  - MIPI Tx (1.0 Gbps/ lane)
  - MIPI Tx on SERDES (2.5 Gbps/ lane)
  - MIPI DSI Tx (1080p60)
  - MIPI DSI Tx (40k60)
- **Image Processing**
  - Alpha Blending
  - Bayer Interpolation
  - Sobel
  - Uncanny Edge Detector
  - Display Controller
  - Image Edge Detection
  - Image Enhancement
  - Image Sharpen
  - RGB to YCbCr
  - YCbCr to RGB
  - Test Pattern Gen
  - Gamma Correction
  - Histogram
  - White Balance
- **Deep Learning Inference**
  - VectorBlox Accelerator SDK v1.3
- **Encode (Decode)**
  - H.264 Partner IP
  - mJPEG compression (PolarFire SoC)
  - H.264 Baseline/ iFrame (PolarFire SoC)
- **DDR Controllers**
  - DDR4/ DDR3/ LPDDR3
  - LPDDR4 Soft Controller
- **Transport Interfaces**
  - CoaXPress 6.25 / 12.5G
  - SDI (HD/3G/12G)
  - 10G MAC / 10G PHY
  - USXGMII (1/2.5/5/10G)
  - HDMI 2.0 Rx / Tx
  - DisplayPort 1.4 Tx
  - USXGMII RSTP demo
  - MIPI Tx on SERDES (2.5 Gbps/ lane)
  - HDMI 2.0 / 1.4 with HDCP 2.0
  - DisplayPort 1.4a with HDCP 2.0
  - USB 2.0, USB3.1 Gen1 & Gen2

Available In-house / Available with Third Party / In Development In-house (Plan)

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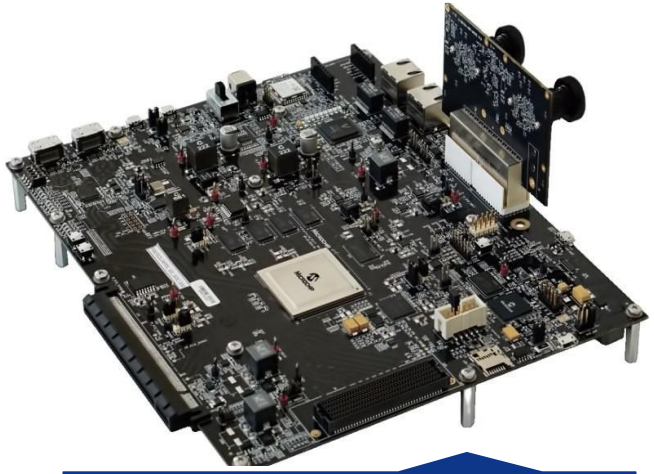
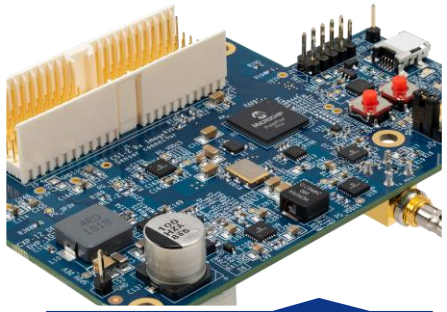
# SEV – Development Platforms



PolarFire SoC Video Kit
**MPFS250-VIDEO-KIT**
Resale $1,838.85

PolarFire Video Kit
**MPF300-VIDEO-KIT-NS**
Resale $1,216.30

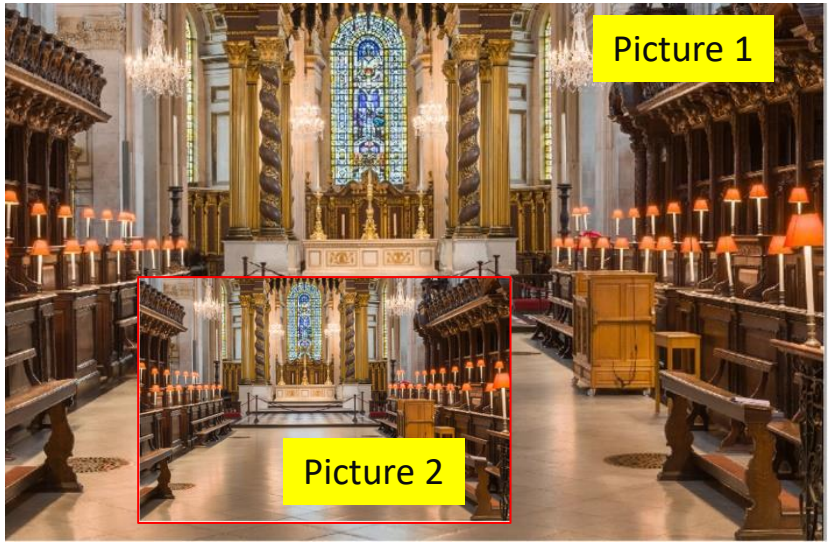


CoaXPress FMC Daughter card
**VIDEO-DC-CXP**
Resale $1,041.76

SDI FMC Daughter Card
**VIDEO-DC-SDI**
Resale $608.82

USXGMII FMC Daughter Card
**VIDEO-DC-USXGMII**
Resale $608.82

# Out-of-Box Demonstrations

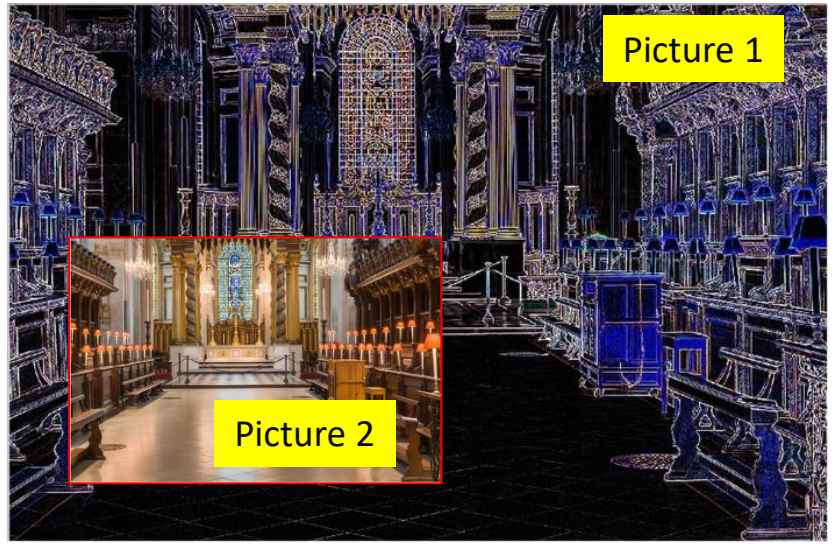


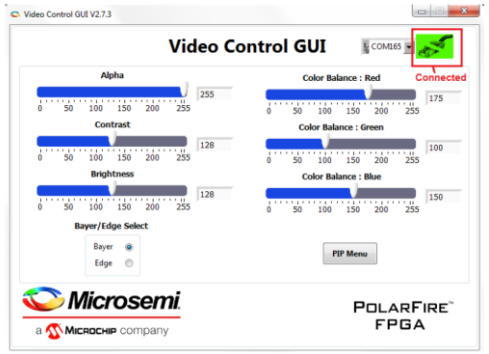

Picture in Picture Demo

← Bayer

Edge Detection →

Picture 1 : 1920 x 1080
Picture 2 : Scaled 1/3



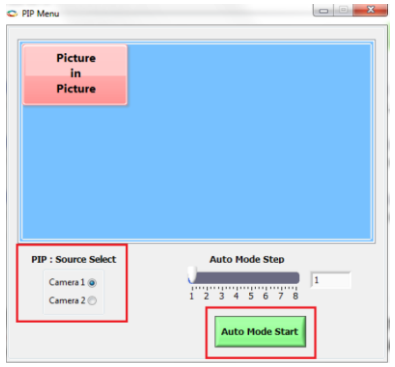




## Video Control GUI

Alpha Blending
Contrast
Brightness
Color Balance: RGB

## PIP Menu

Select Source
Choose movement speed

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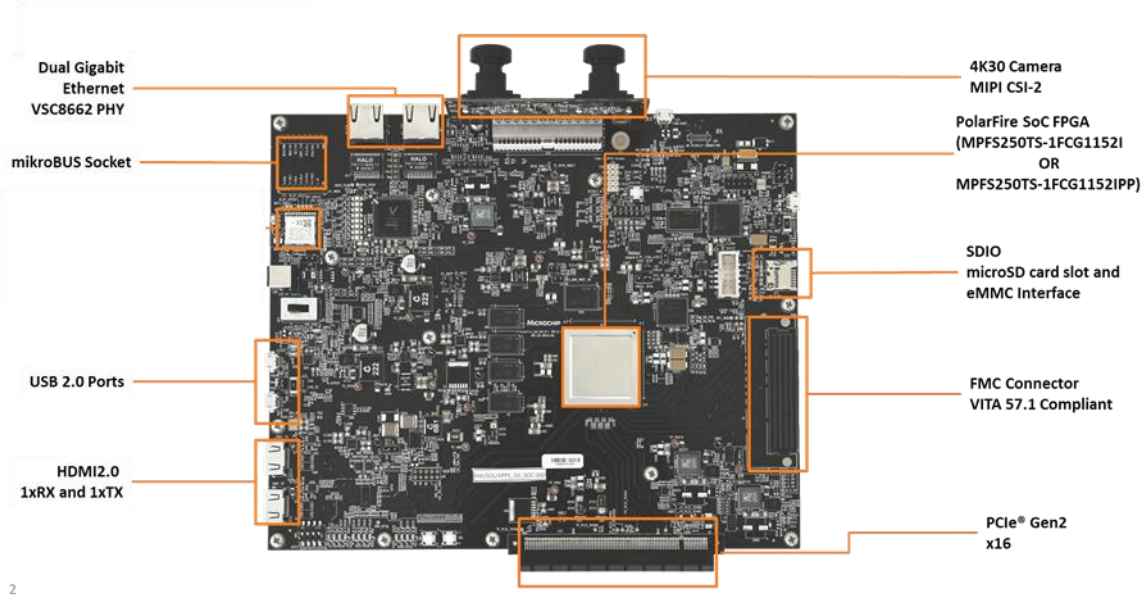
# The PolarFire® SoC Smart Embedded Vision Kit

## Feature List

| | |
|---|---|
| **General Information** | PolarFire SoC FPGA (MPFS250TS-1FCG1152I)<br>SiFive E51 Monitor core (1 x RV64IMAC) , SiFive U54 Application cores (4 x RV64GC), and Secure boot |
| | Sony 4K Dual Camera Sensors (IMX334) |
| | CE , RoHS |
| **Program and Debug** | Onboard JTAG/ or (multiplexed)<br>Onboard embedded FlashPro |
| **Memory and Storage** | 4GB DDR4 x64 |
| | 2GB LPDDR4 x32 |
| | 1Gb SPI Flash |
| | 8 GB eMMC flash & 16GB SD card slot (multiplexed) |
| **User Defined I/O** | 4x LEDs |
| | 4x User Push buttons |
| | 1x DIP Switch (x4) |
| **Expansion Connectors** | 1x VITA 57.1 HPC FMC |
| | PCIe® Gen2 x16 |
| | 1x Mikrobus socket |
| **Communication & Networking** | 4x UART (via USB Bridge) |
| | 1x CAN-FD Header |
| | 2x GbE RJ-45 Connectors |
| | 1x microUSB High speed USB 2.0 OTG |
| | 1x I2C (via USB bridge) |
| **Imaging and Video** | HDMI2.0 Video Output |
| | HDMI2.0 Video Input |
| | MIPI DSI Output |
| | MIPI CSI-2 Input |
| **Clocking** | 50MHz MEMS Oscillator |
| **Power** | 12V DC Supply |




Expected availability in Dec 2022



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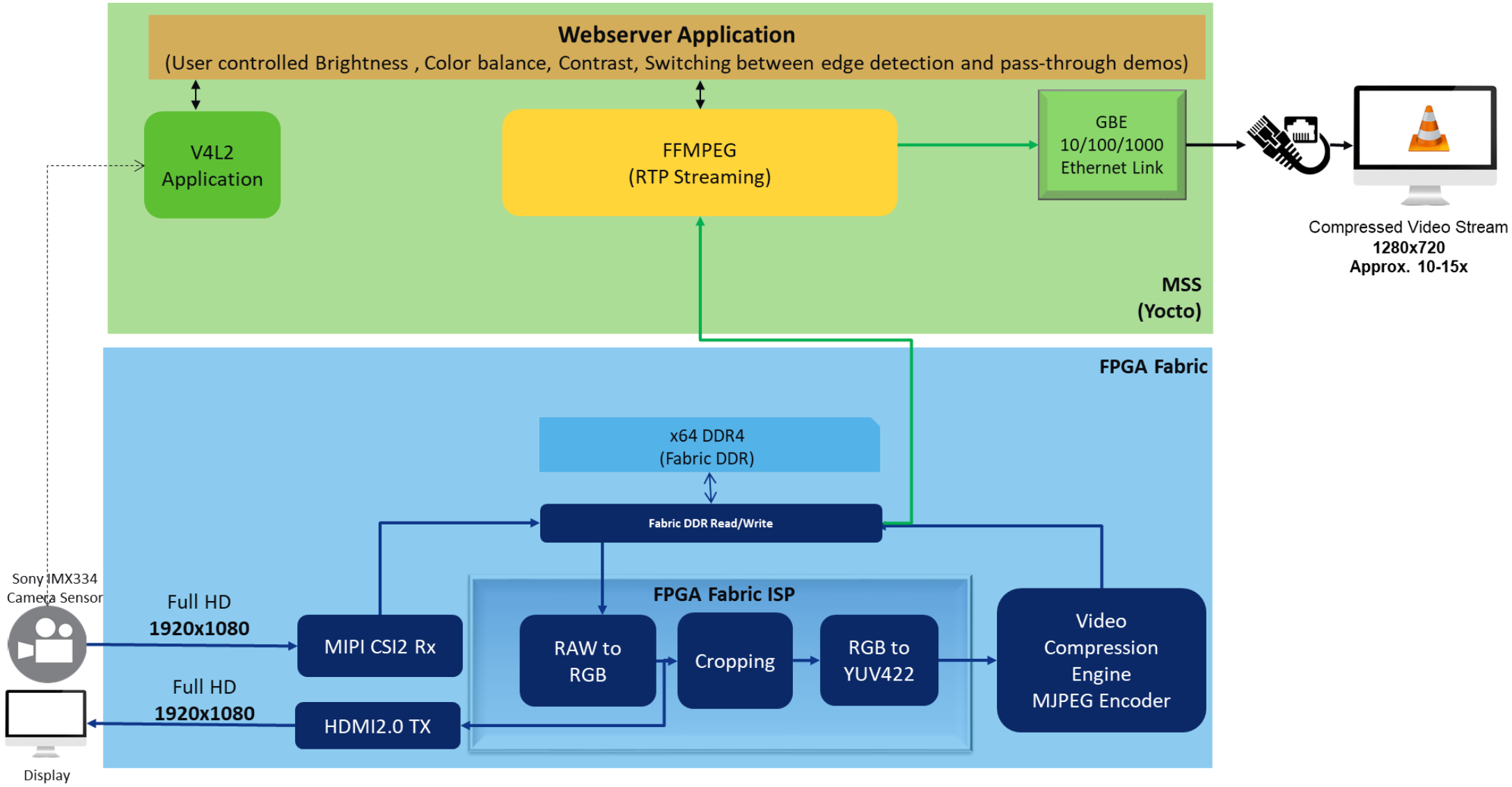
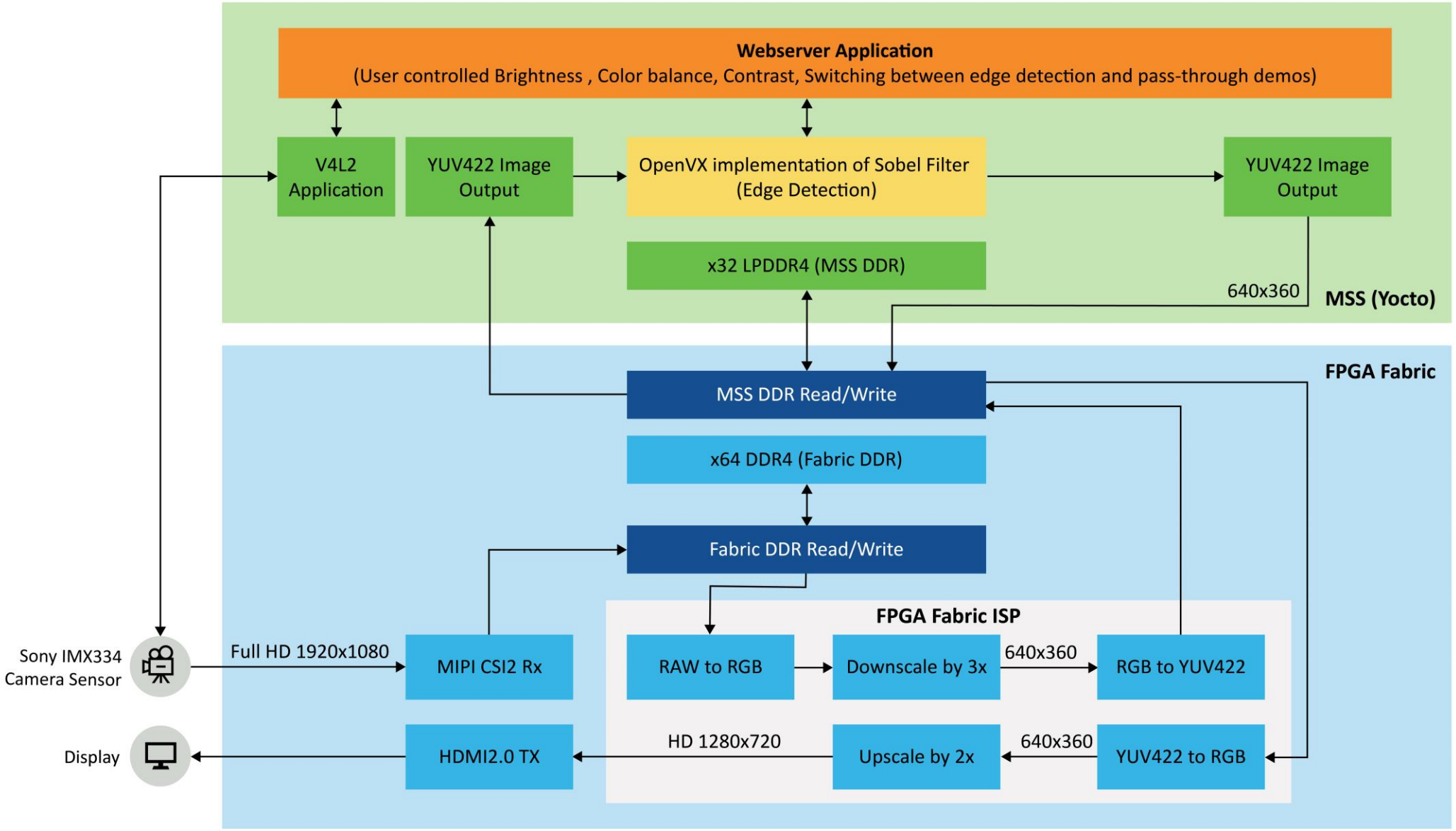
# MJPEG Compression – OOB, Pre-programmed



# Sobel Filter using OpenVX

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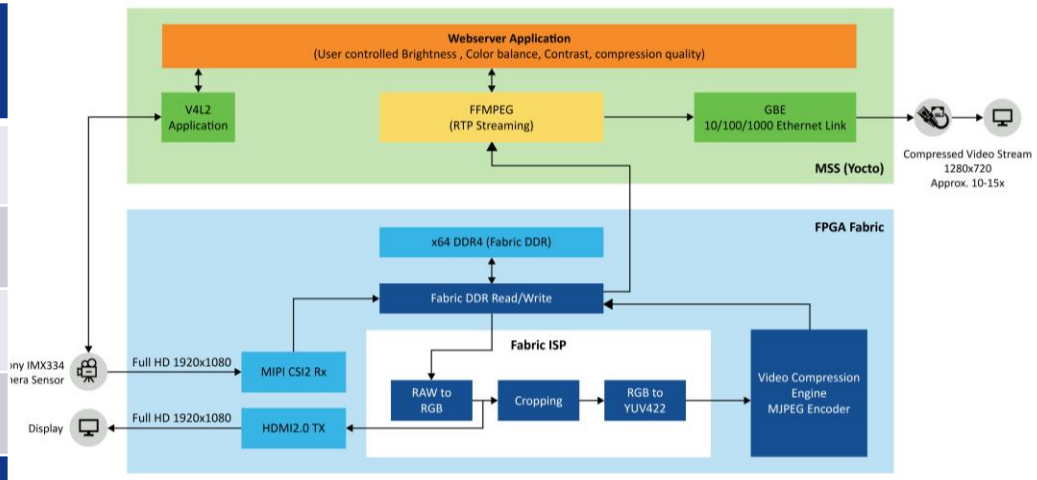
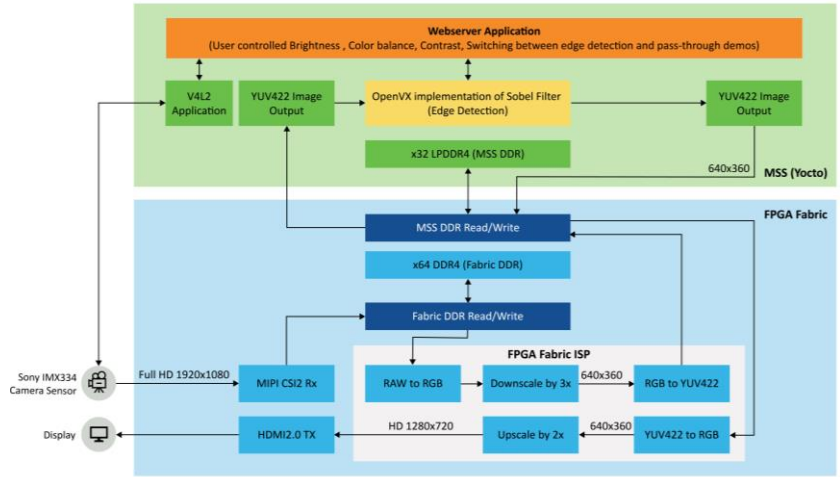
# Solutions Plan

| # | Solutions (App Note + tcl+ Job File + WIC) | Planned Availability | | Platform |
|---|---|---|---|---|
| | | Internal release | w/PP kit launch | |
| 1 | MIPI CSI-2 -> ISP -> mJPEG -> 1G Interface | Apr'22 | May'22 | GitHub MCHP Web |
| 2 | MIPI CSI-2 -> ISP -> H.264 -> 1G Interface | Apr'22 | May'22 | GitHub MCHP Web |
| 3 | MIPI CSI-2 -> OpenVX Edge Detection -> HDMI out | Apr'22 | May'22 | GitHub MCHP Web |
| 4 | MIPI CSI-2 -> Picture in Picture -> Edge Detection -> HDMI out (Baremetal) | Apr'22 | May'22 | GitHub MCHP Web |
| **Solutions in the Pipeline** | | | | |
| 5 | MIPI CSI-2 -> ISP -> HDMI out / MIPI DSI Display out | | Jun'22 | |
| 6 | MIPI CSI-2 -> Open VX based Face Detection | | FY23Q3 | |
| 7 | VectorBlox in PolarFire SoC | | FY23Q3 | |
| 8 | I2S (MSS) -> OPUS Audio Decoding (Fabric) | | FY23Q2 | |
| 9 | OpenVX Stereo Vision | | FY23Q2 | |
| 10 | IoT Cloud Connectivity for OTA/ Meta Data Upload | | TBD | |
| 11 | SmartHLS in PolarFire SoC specific to Smart Embedded Vision | | FY23Q2 | |
| **On-Demand Demonstrative Designs** | | | | |
| 12 | CoaXPress Solution | | | On-Demand |
| 13 | MIPI CSI-2 -> Serial Digital Interface | | | On-Demand |
| 14 | MIPI CSI-2 -> USXGMII | | | On-Demand |

**mJPEG Compression**




**OpenVX demo in MSS**

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# PolarFire Imaging DirectCores (VDSOLCores)

## Availability

| Core Name | Obfuscated | RTL | Current Availability |
|---|---|---|---|
| Core10GMAC | $10,000 | Not Available | Available |
| CoreUSXGMII | Free with Libero SoC Software | $10,000 | |
| Core10GBaseR_PHY | | Not Available | |
| SDI (SD/3G/HD/UHD) | | Not Available | |
| CoaXpress (upto 12.5Gbps) | | $5,000 | |
| MIPI CSI-2 Tx/Rx | | $5,000 | |
| SLVS EC Rx (RAW8, 2 lanes) | | $10,000 | |
| Alpha Blending | | $1499 (Bundle) | |
| Bayer Conversion (1080p, 4K) | | | |
| Color Space (YCbCr/ RGB) | | | |
| Display Enhancement (Brightness/Contrast/Hue) | | | |
| Display Controller (1080p, 4K) | | | |
| HDMI Tx/Rx | | | |
| Image Enhancement | | | |
| Image Edge Detection | | | |
| Image Sharpen | | | |
| Pattern Generator | | | |
| Scaler | | | |
| Video DMA (DDR Memory Arbiter) | | | |

# Smart Embedded Vision IPs from 3rd Party

| Core Name | Price | Vendor |
|---|---|---|
| HDMI Rx, Tx 2.0 | $15K | Bitec |
| HDCP 2.2 | $45K | Bitec |
| Display Port 1.4a | $19,995 | Bitec |
| SATA 2.0 | $25K (Netlist) / $75K (Source) | ASIC Design Services |
| Crest Factor Reduction | Depends on customer requirements | Systems4Silicon |
| Digital Pre-distortion | Depends on customer requirements | Systems4Silicon |
| H.264 Encoder | Baseline, light motion estimation: $40K<br>Baseline, full motion estimation: $48K | Alma Technologies |
| USB 3.1 Gen2 (10 Gbps) and Gen1 IP (5 Gbps) | Negotiable with Customer (~$35K) | Corigine |
| | Negotiable with Customer (~$20K) | SLS |

# SEV Success Stories

Portable Ultrasound

MRI Machine

10G Ethernet Cam

SDI Conversion

Telescopic Cameras

SDI Camera

CoaXPress Camera

Night Vision Goggles
Smart Glasses

Endoscope Camera

Robotic Stereo Camera

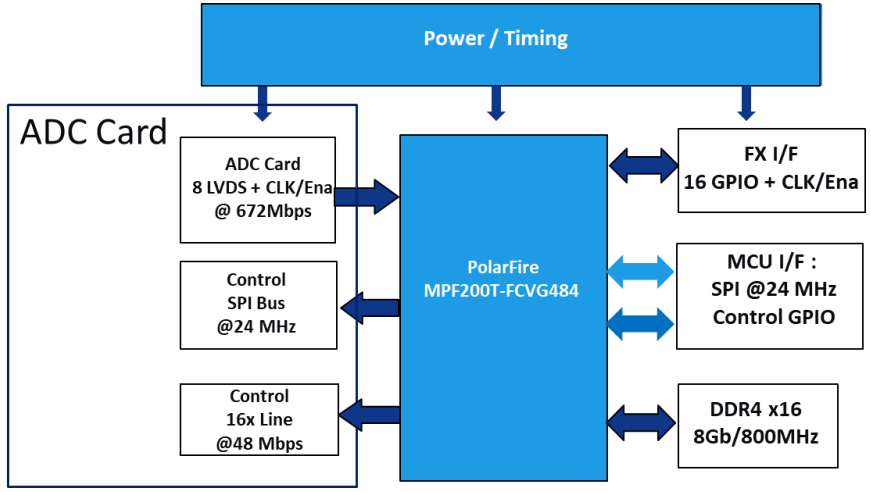
Microscope Cameras

Thermal Cameras

MICROCHIP

# Portable Ultrasound

- **Requirements for PolarFire**
  - Low Power - Battery operated
  - MPF200TL- FCVG484E
    - Using Power Screened Parts
  - IOs CMOS  -> GPIO and SPI bus/control I/F
  - DDR4 x16 @ 800 MHz
  - LVDS IF @ 672 Mbps to ADC Card
- **Requirements for PolarFire SoC**
  - Cable-less communication over Wi-Fi
  - Wi-Fi stack running on RTOS

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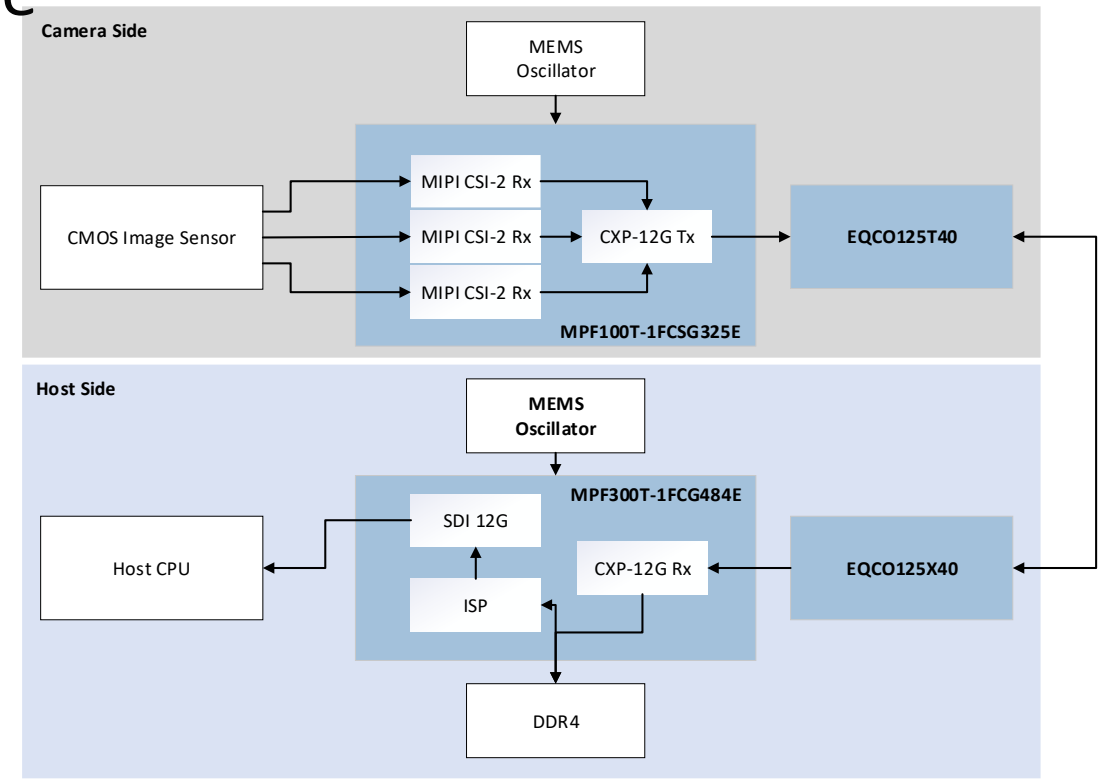
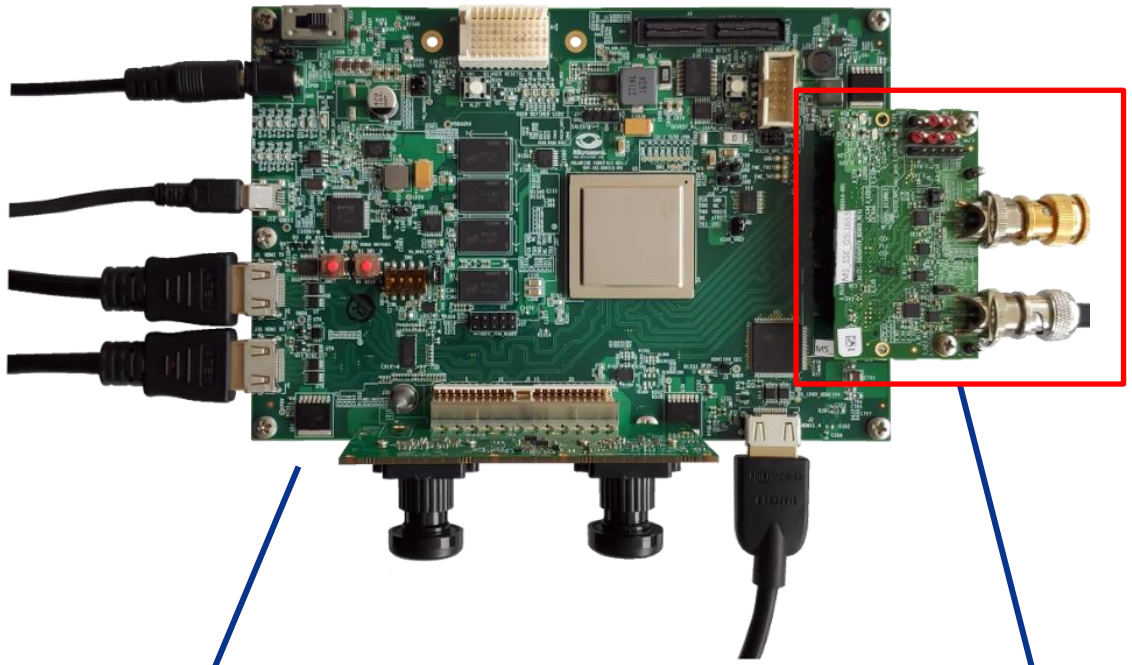
# Endoscope Camera using CoaXPress 12G

- **Requirements for PolarFire**
  - Small Form Factor: MPF100T-1FCSG325E
  - Enable 12 Gbps delivery using single cable
  - Lowest power requirement at camera head
  - Temperature below 45C during operation



# Key SEV IP Details

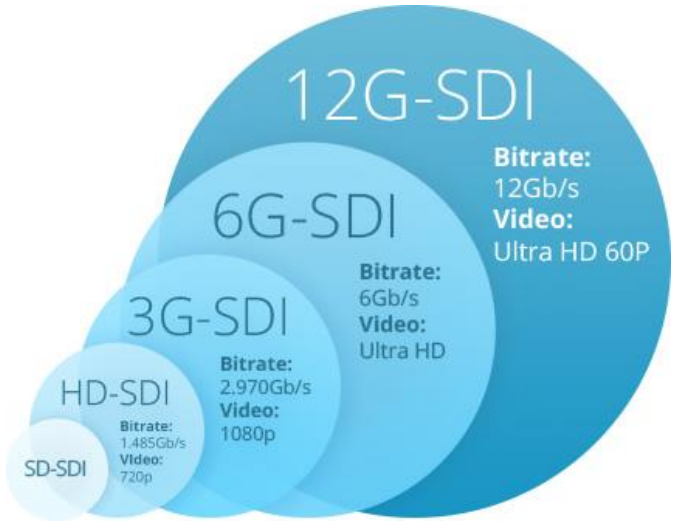
# Serial Digital Interface - FMC



MPF300-VIDEO-KIT-NS

SDI FMC*

| Part Number | List |
|---|---|
| VIDEO-DC-SDI | 499 |




- Supports 6G and 12G data rates
- Society of Motion Picture and Television Engineers (SPMTE) compliant IP Cores
- SDI Rx and Tx IPs in Libero Catalog

FMC - FPGA Mezzanine Card or Daughter Card
Connects to a High-pin-count FMC adapter on FPGA eval boards

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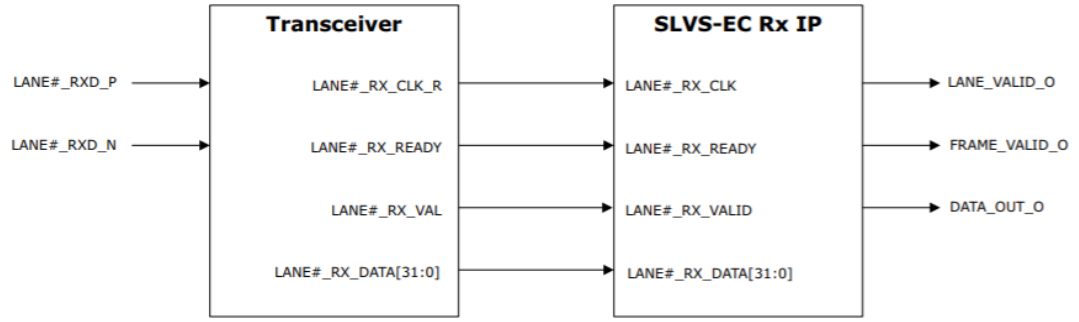
# HDMI Bitec vs. In-house Offering

| | Bitec (3rd Party IP Partner) | In-house |
|---|---|---|
| **Resolution** | Rx: 4K@60<br>Tx: 4k@60 | Rx 1080p@60 (now), 4K support later<br>Tx 4K@60 |
| **Compatibility** | HDMI 2.0b, 1.4 | HDMI 2.0b and 1.4 |
| **Color-depth** | 8,10,12 & 16 bit | 8 bit |
| **Pixel per clock** | Tx: 1-,2- or 4- symbol/pixel per clock input/output<br>Rx: 1-,2- or 4- symbol/pixel per clock input/output | Tx: 1-, 2-, 4- pixel per clock<br>Rx: 1- pixel per clock |
| **Color format** | Supports RGB, YCbCr Colorimetric Formats | Supports RGB |
| **Audio channels** | 2-, 8 and 32-channel Audio support | No Audio support |
| **Audio formats** | 3D and MST Audio support | No Audio support |
| **Raw aux** | Raw auxiliary data stream output & input | No auxiliary data stream support |
| **Transceiver integration** | Seamless interface to device transceiver | Transceiver is not included within the IP, the IP has to be connected to transceiver in Libero |
| **CEC** | Optional CEC 1.4 and 2.0 support | No CEC support |
| **HDCP** | Optional HDCP 1.4/2.3 support | No HDCP support |
| **Pricing** | ~$15,000 USD | Rx/ Tx Obfuscated: Free with all Libero*<br>Rx/ Tx RTL: Part of ISP Bundle* |

# SLVS-EC Receive IP

- **Features**
  - Up to 2 lane SLVS-EC v1.2
  - RAW 8 date type
  - Free with Libero Gold
  - In development
    - Up to 8 lane SLVS-EC
    - RAW 8/10/12
    - SLVS-EC v2.0 (4.7 Gbps per lane)

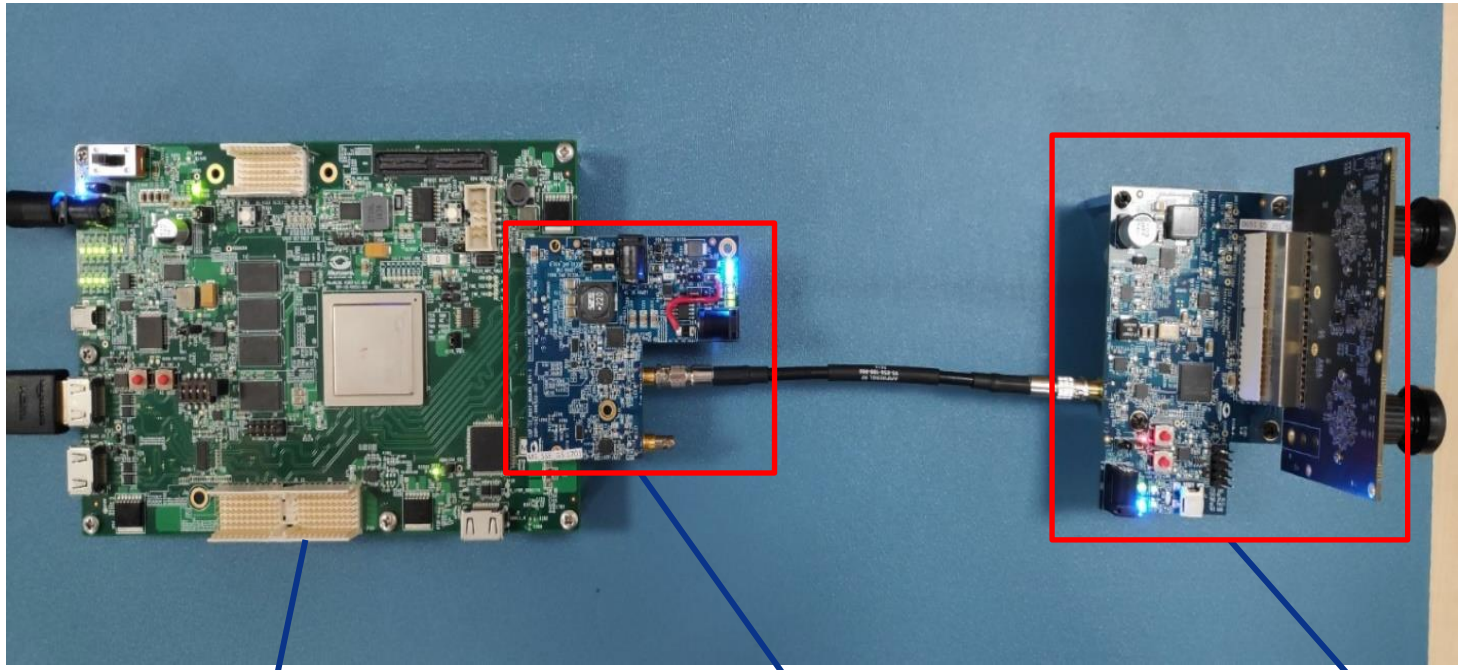



| Element | Usage |
|---|---|
| DFFs | 1645 |
| LUT-4 | 1020 |
| LSRAMs | 13 |

MICROCHIP

# CoaXPress 6.25 and 12.5 Gbps

- Supports 6.25/12.5 Gbps Rx/ Tx
- Uses Microchip EqcoLogic 12.5 Gbps CoaXpress PHYs



| Part Number | List |
|---|---|
| VIDEO-DC-CXP | 849 |

MPF300-VIDEO-KIT-NS

MPF300T

CoaXPress FMC

EQCO125Rx
EQCO125Tx

CoaXPress DEVICE

MPF100T
EQCO125Tx

MICROCHIP

# Introduction to Deep Learning Inference

Machine Learning with PolarFire

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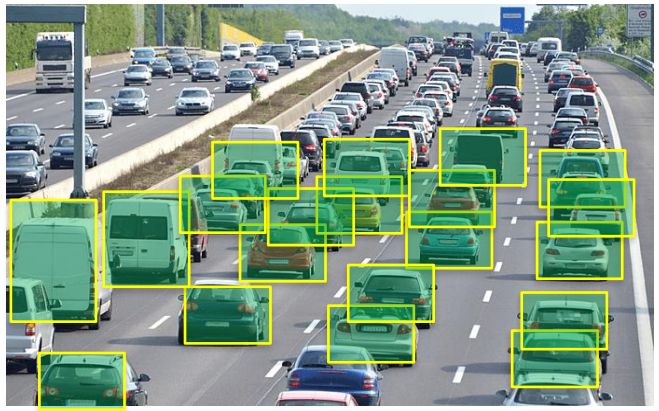
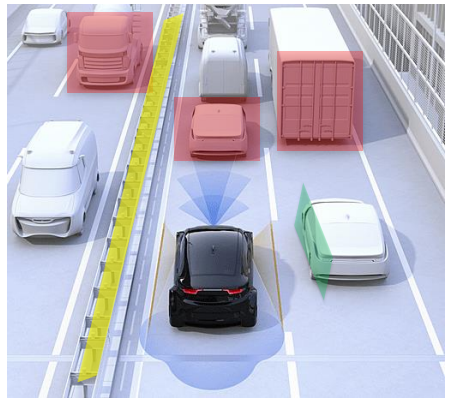
# Inference in Embedded Vision



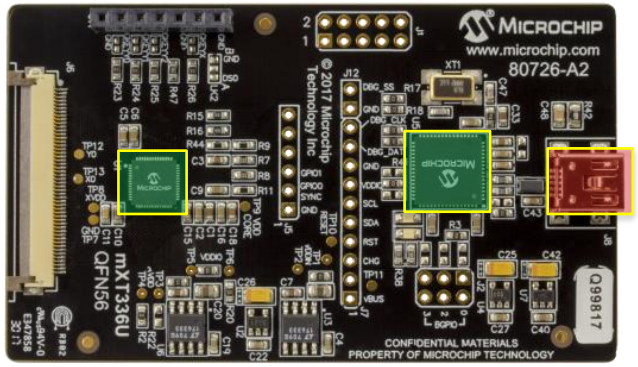
Traffic Monitoring


Machine Vision



Autonomous Driving

Surveillance

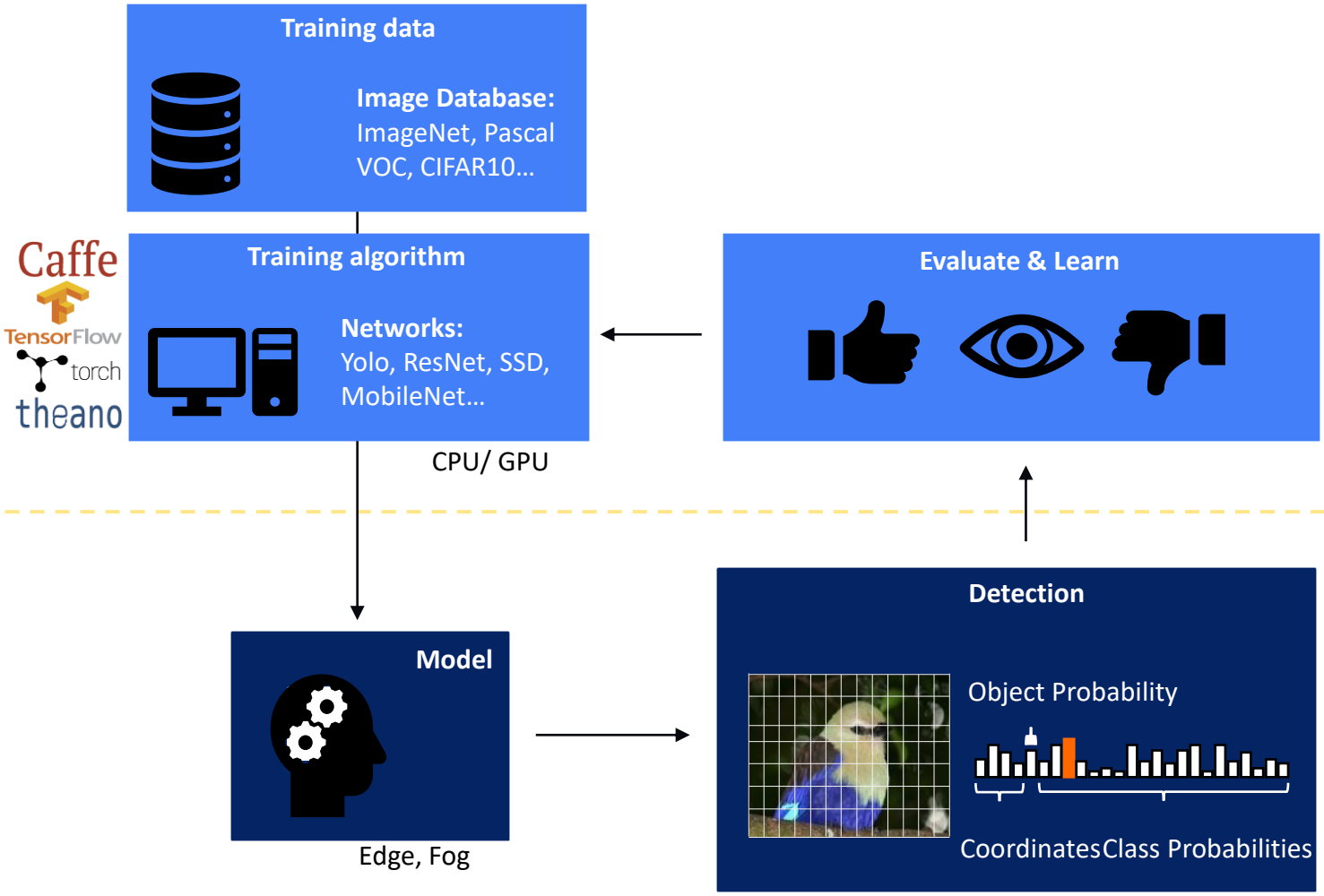



PCB Inspection

Drone Vision

MICROCHIP

# The Deep Learning Construct




## Network Training

- In the data centre or workstation
- Large compute capacity
- No power or space constraints

## Inference

- Need Low Latency
- Power & space constrained
- Requires security and reliability

# Introducing VectorBlox Accelerator SDK and Neural Networking Solution

In Development

Broad Launch September 2020

Early Access July 2020

# Addressing FPGA Development Challenges

## Models developed in the software domain

Network

RTL

VHDL VERILOG

## Many frameworks used by AI/ML developers

TensorFlow

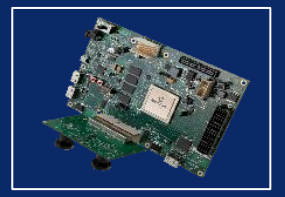
MathWorks

ONNX

Caffe2 PYTORCH Chainer

mxnet CNTK PaddlePaddle

## Need out-of-box evaluation platforms



Smart Camera

PCIe Interface

## Enable evaluation before choosing hardware

Network

Simulator


FPGA

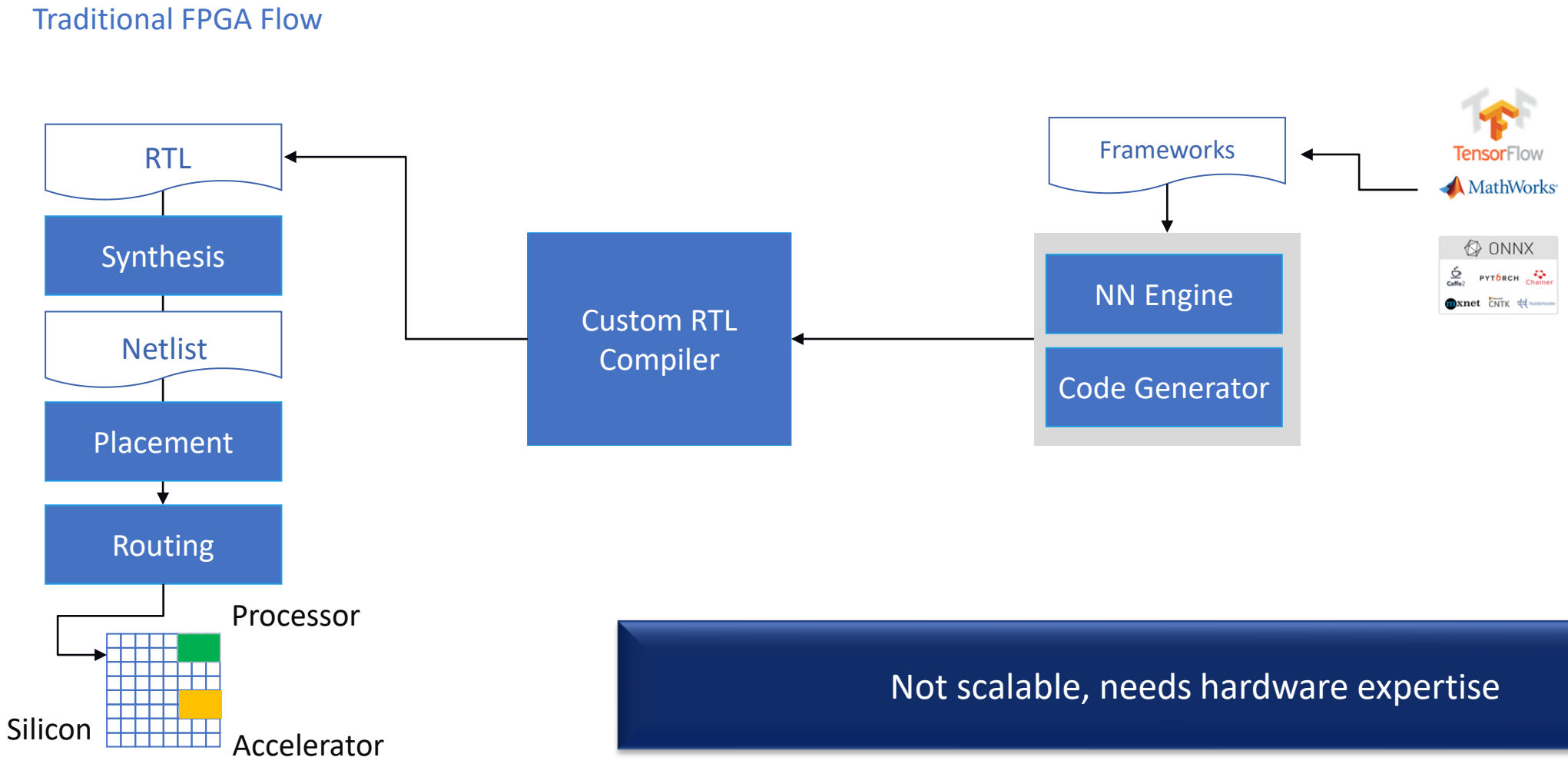
## Translating models into RTL requires expertise

## Custom Implementation for each framework

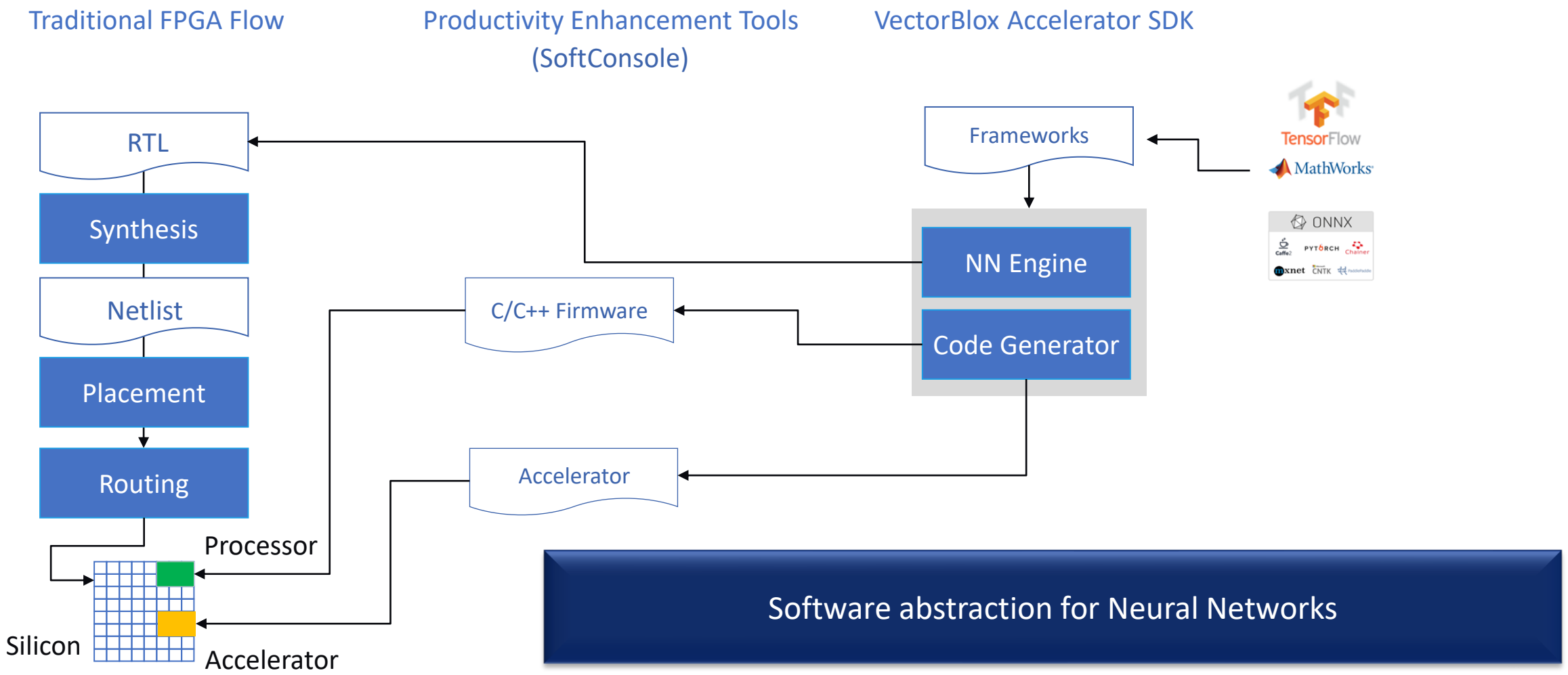
## Learning curve for new developers

## Validate CNNs before investing in hardware

# Traditional FPGA Design Flow Challenges



# Traditional FPGA Design Flow Challenges

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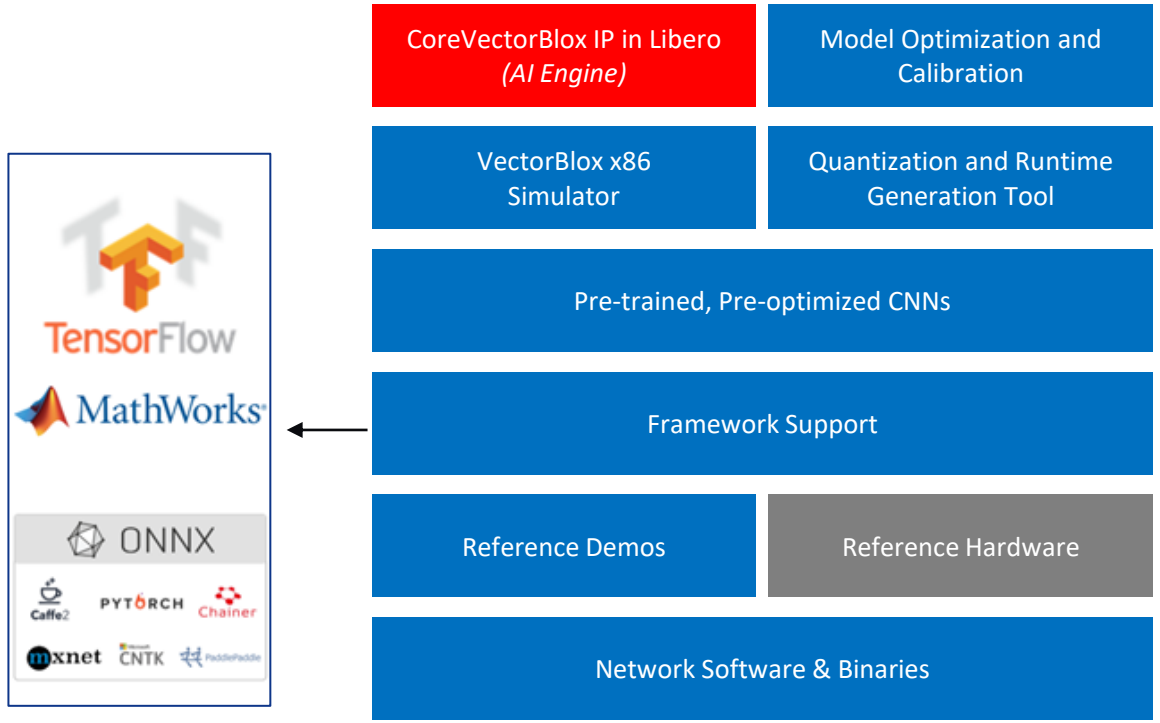
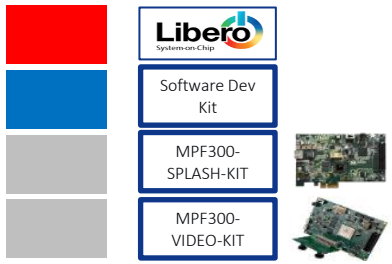
# VectorBlox™ Accelerator Software Dev Kit

- Enables developers to code in C/C++ and use power efficient neural networks
  - No prior FPGA design experience required.
  - Works on Linux and Windows.
- Executes models in TensorFlow and ONNX
  - Offers the widest framework interoperability
- Includes a bit accurate simulator
  - Users can validate the accuracy of the hardware while in the software environment.
- Pre-trained Neural Networks demos included
  - Users can load different network models at run time on supported hardware

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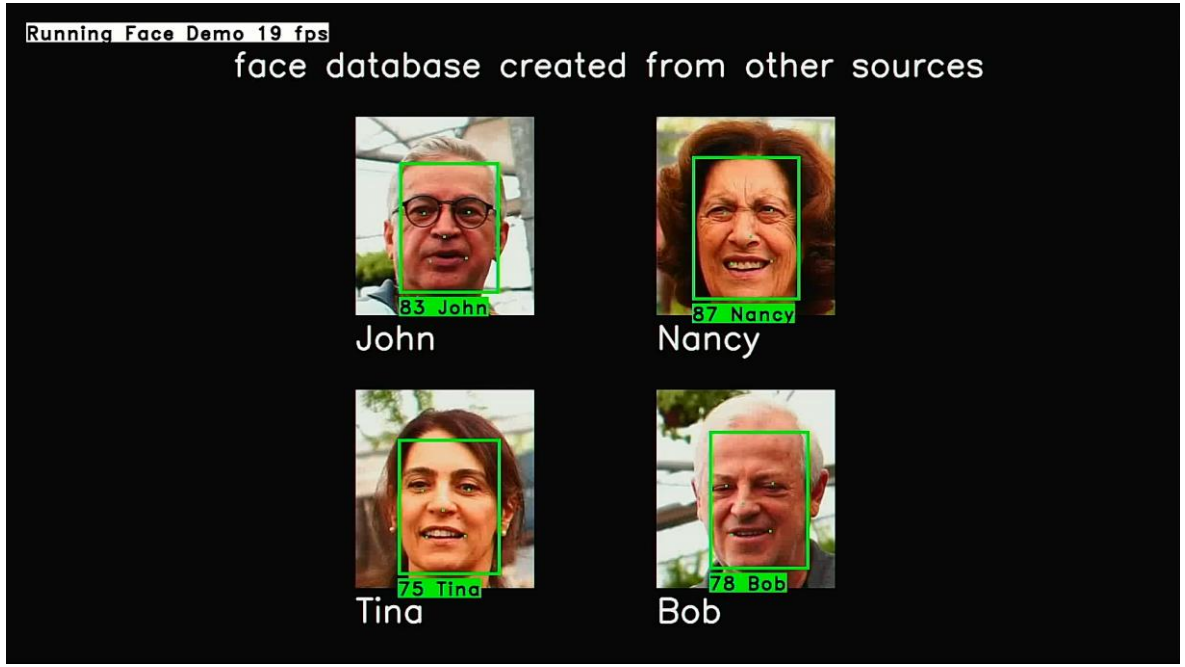
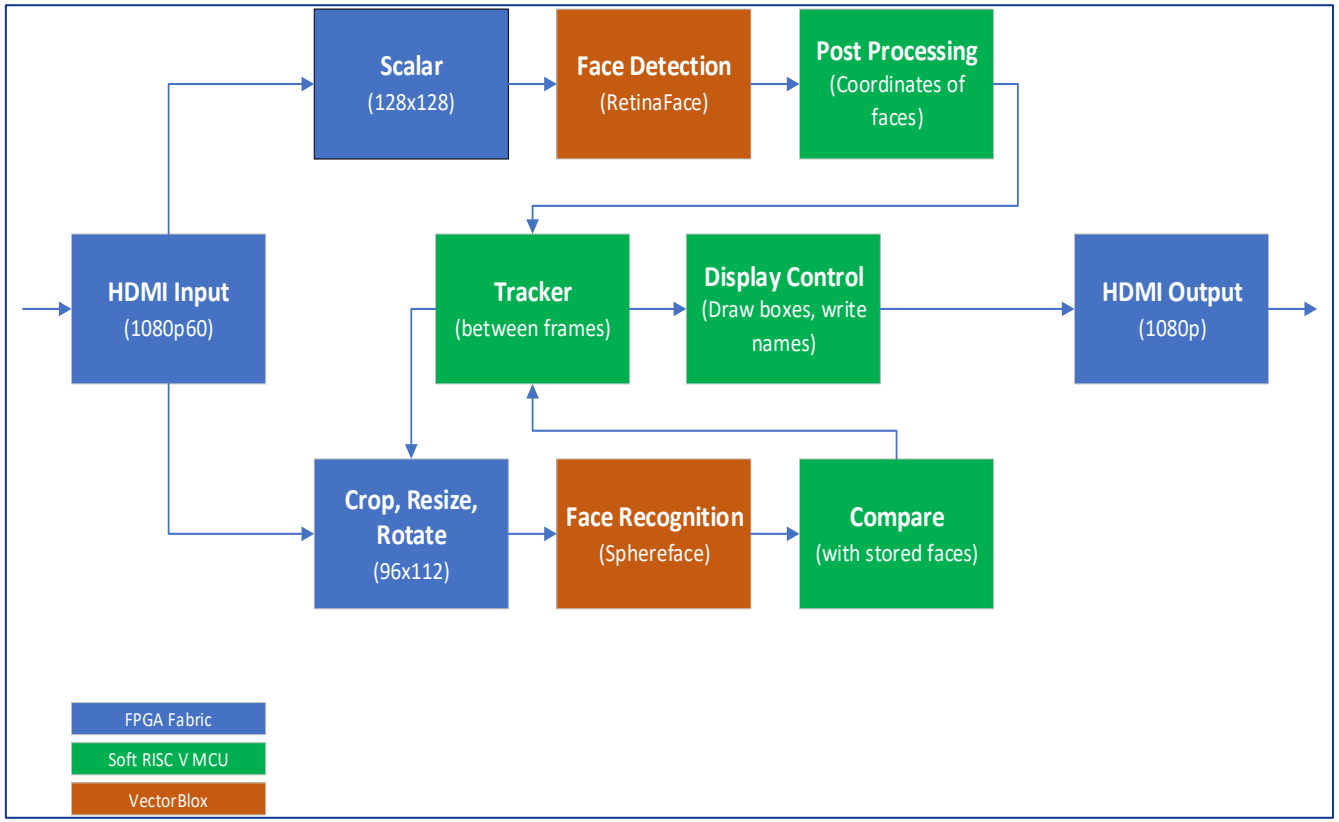
# Solution Demo: Facial Recognition



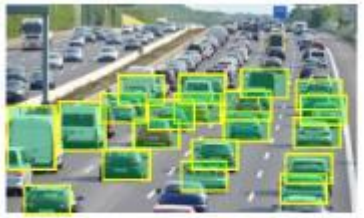




- Pipelining Retinaface (detect face) and Sphereface (map face)
- Opensource models trained in Pytorch

# Thank You

# VectorBlox Neural Network Engine Tool Kit

- New Design Flow enables software developers to evaluate AI solutions
- Evaluation platform can be deployed with limited FPGA knowledge

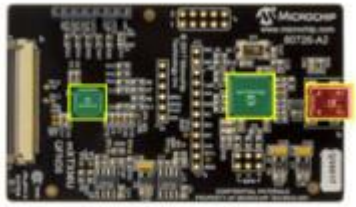


Traffic Monitoring

Machine Vision

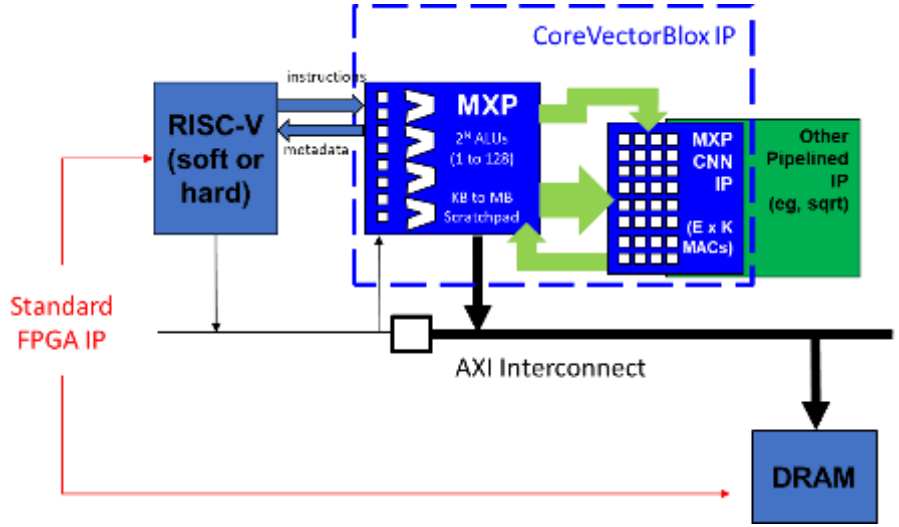
ADAS

Surveillance



PCB Inspection

Drone Vision

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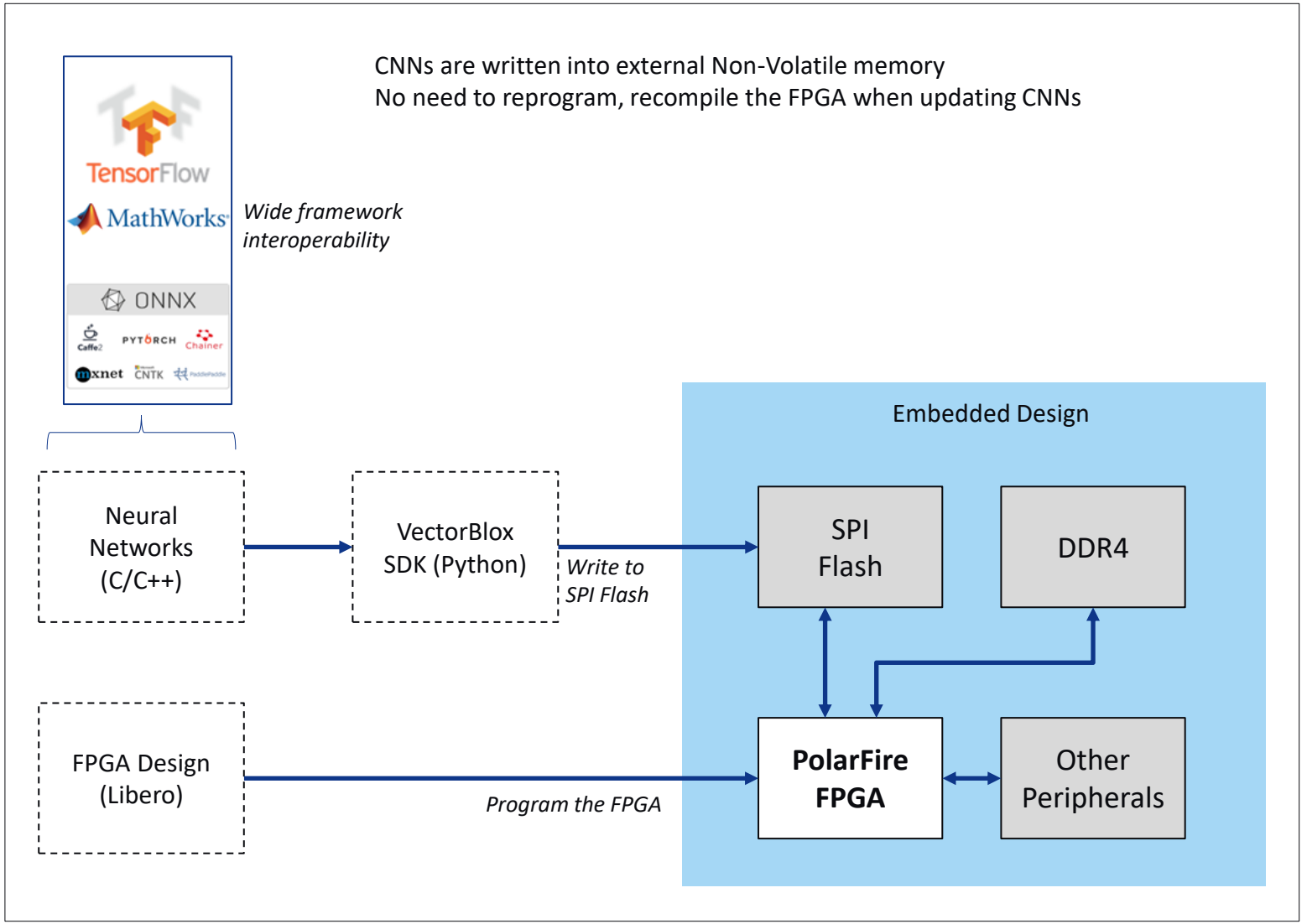
# VectorBlox SDK




- C/C++ based CNN control
- Wide framework support- TensorFlow, Caffe, PyTorch, Mxnet, ONNX…
- Includes a bit accurate simulator
- Model zoo for pre-trained CNNs and tutorials

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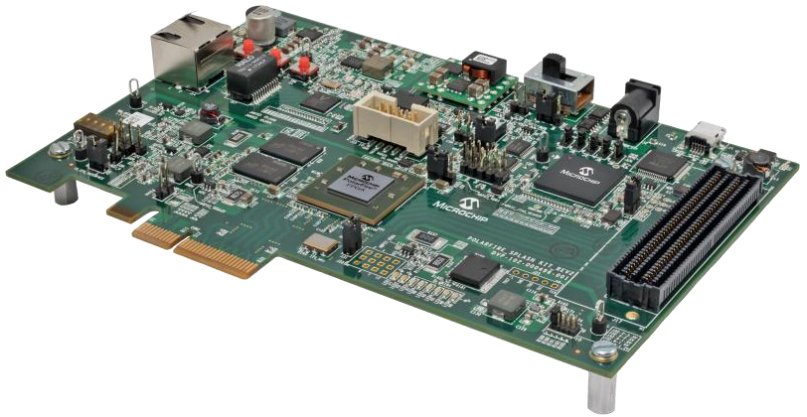
# VectorBlox™ Solutions

HDMI In

MIPI CSI-2 In

PolarFire® FPGA Video Kit

PCIe In, PCIe Out



PolarFire® FPGA Splash Kit

HDMI Out

VBX 1.0
Tiny Yolo v3, ResNet 50, MobileNet v1

VBX 1.2
Facial recognition

License plate detection

Webpage: https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-design-resources/vectorblox-accelerator-software-development-kit
Mail: vectorblox@microchip.com

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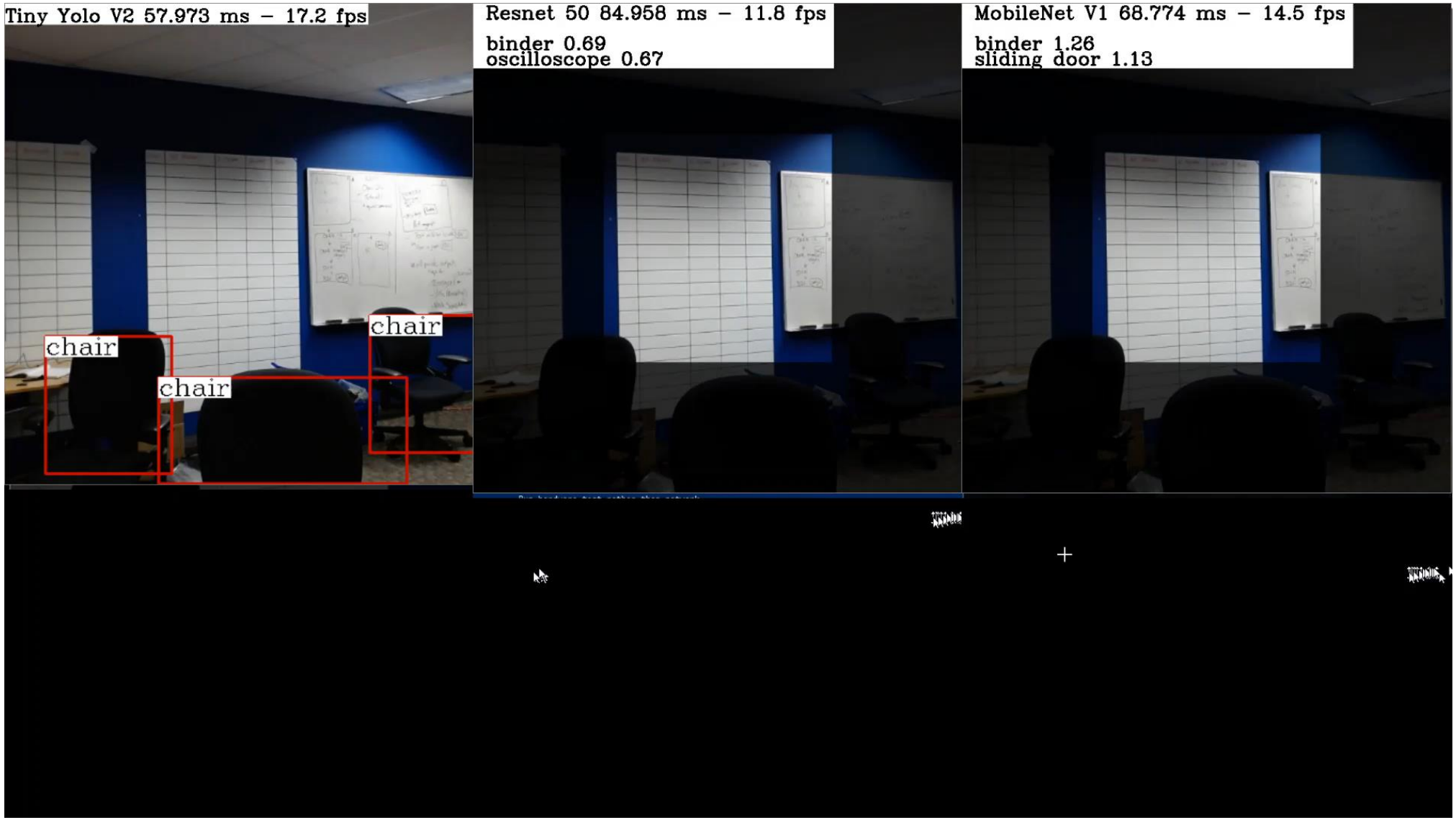
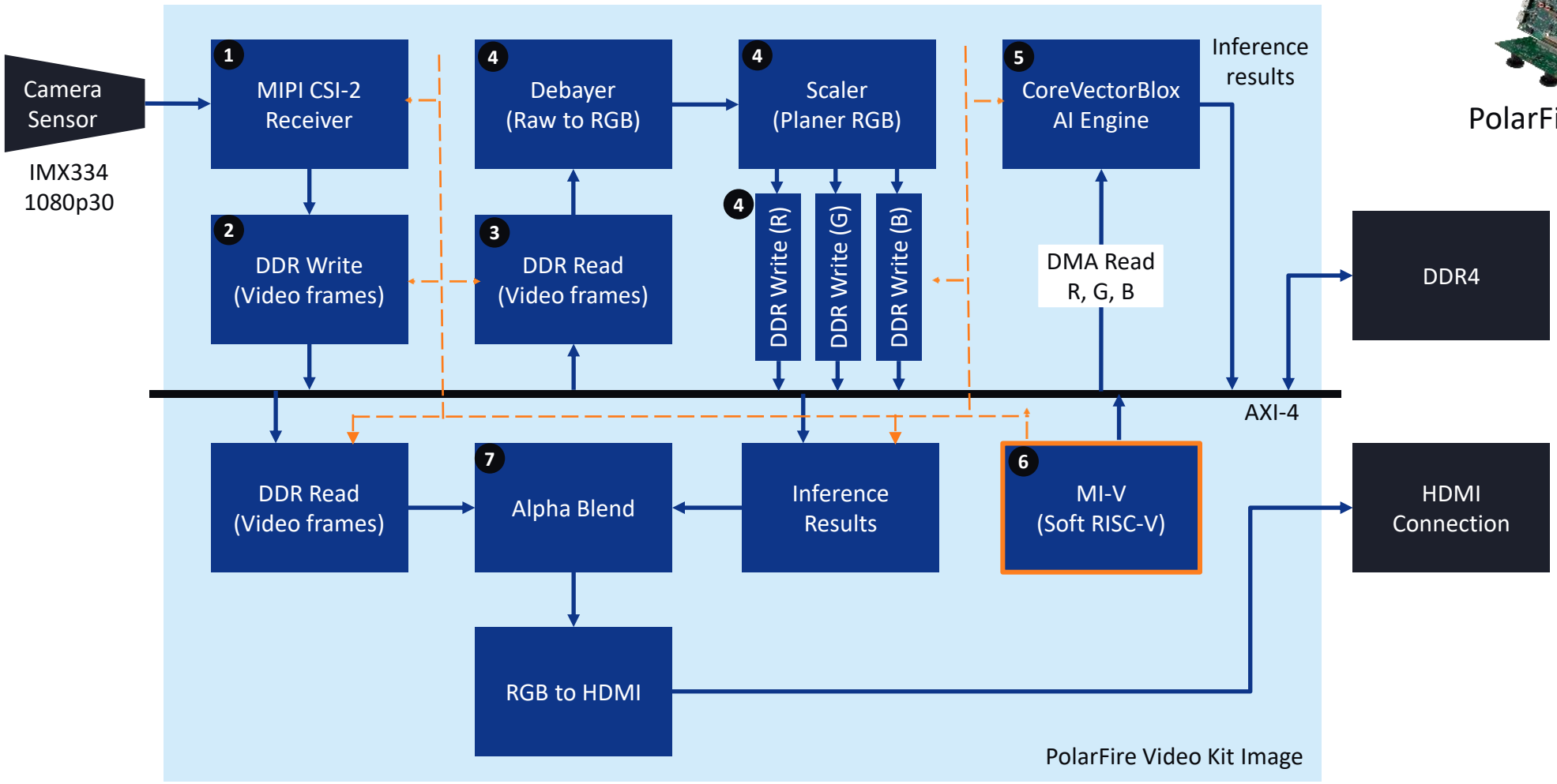
# Processing Single Stream Sequentially



# Switching CNNs on a single stream

PolarFire Video Kit




1. Video frame is received via MIPI CSI-2
2. And stored in the DDR via AXI-4 interconnect
3. Before inference – the frame is read back from the DDR
4. Converted from RAW to RGB, RGB to planer R, G, B and written back into DDR
5. CoreVectorBlox engine runs inference on R, G, B arrays and writes results back into DDR
6. Mi-V sorts probabilities, creates an overlay frame with bounding boxes, classification results, fps etc. and stores the frame in DDR
7. The original video frame is read and blended with the overlay frame and sent out to an HDMI display

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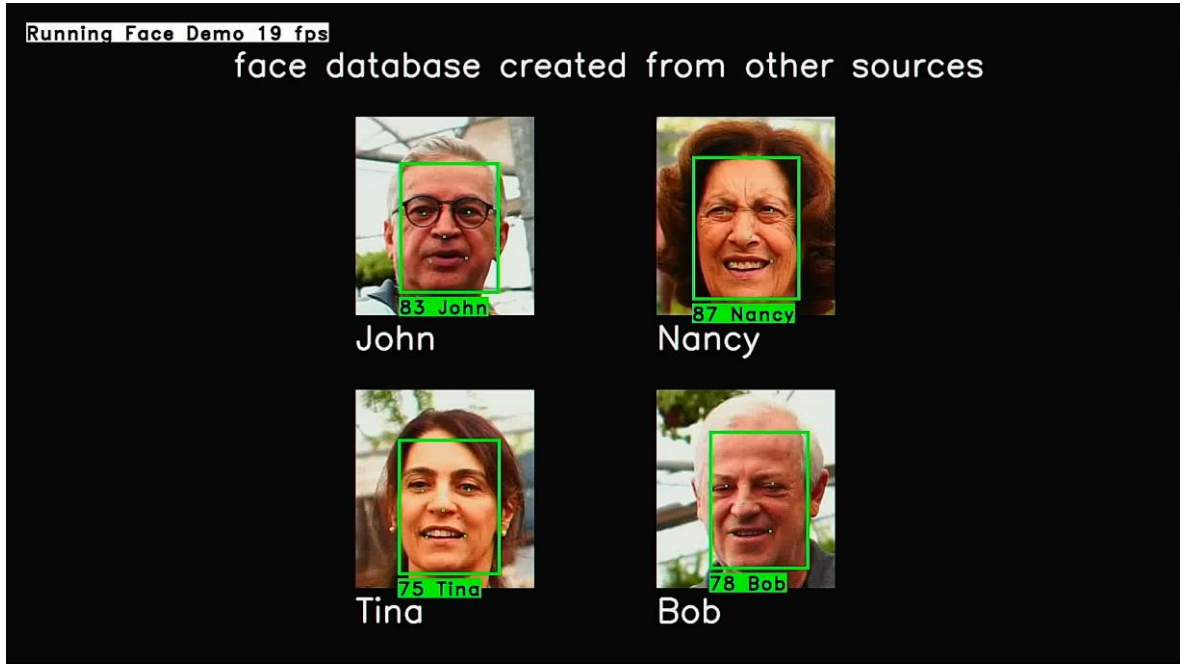
# Solution Demo: Facial Recognition

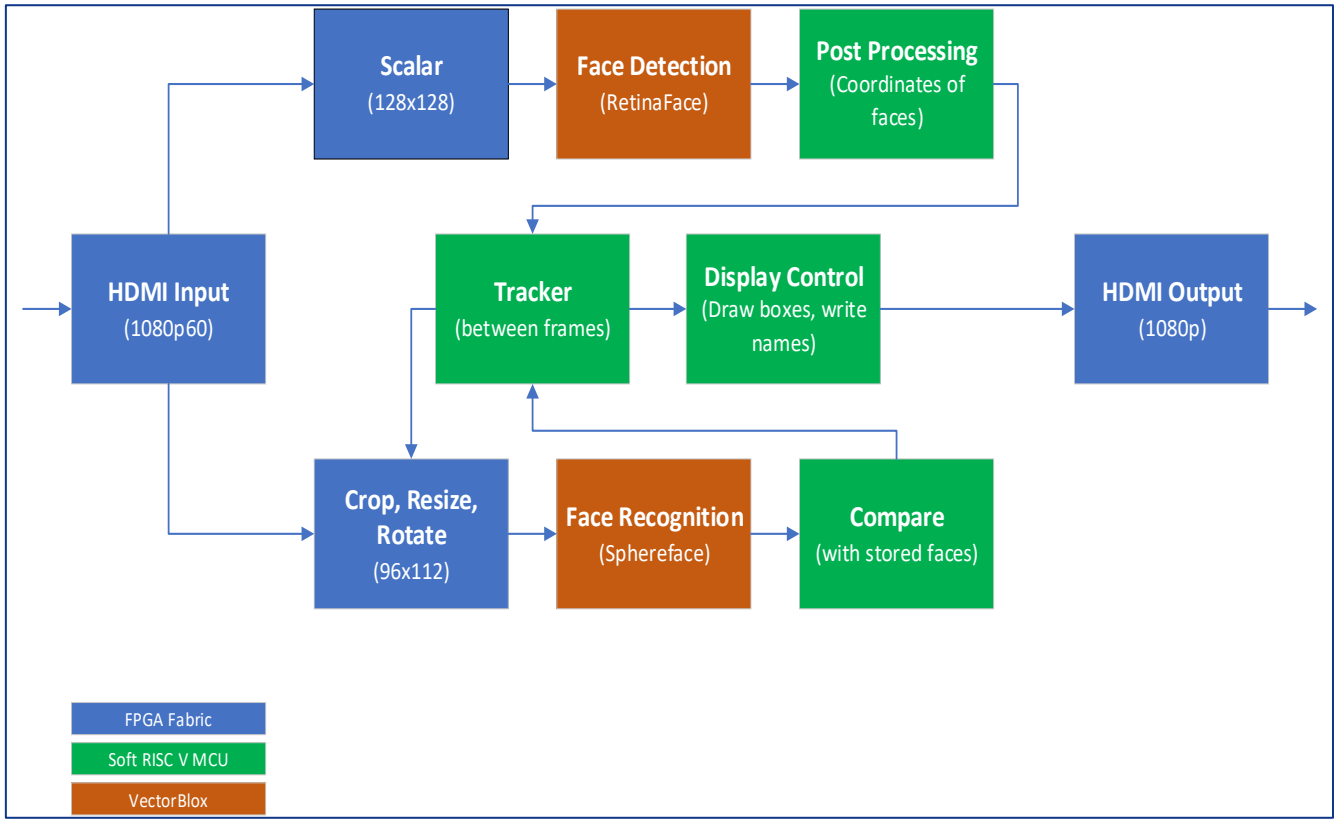
- **A two-step process, 2 CNNs with one Accelerator**

- **First RetinaFace MobileNet**
  - Used in mobile apps
  - 0.5GOPs with 430K parameters
  - Multi outputs
    - Bounding box
    - Eyes, nose, mouth
    - Confidence value

- **Second SphereFace**
  - 3.5GOPs with 22M parameters
  - Runs on each face detected by BlazeFace
  - Input 112x96 image (produced from BlazeFace bounding box)
  - Output is a 512 element vector
  - 512 vectors are compared to the vector of known faces
    - Person of interest photo is run through SphereFace to build a known face vector

# Solution Demo: Facial Recognition



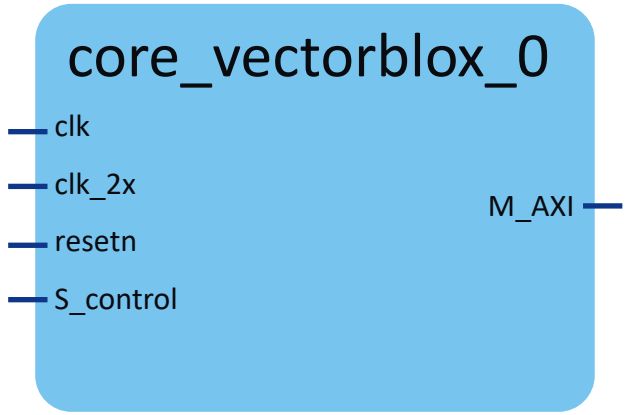

- Pipelining Retinaface (detect face) and Sphereface (map face)
- Opensource models trained in Pytorch

# CoreVectorBlox v1.3 Utilization and Performance

| Resources | V250 | V500 | V1000 |
|---|---|---|---|
| Peak GOPs | 79 | 146 | 279 |
| ResNet-50 (fps) | 4 | 8 | 14 |
| Tiny Yolo v3 (fps) | 5 | 10 | 28 |
| MobileNet v1 (fps) | 19 | 38 | 81 |
| MobileNet v2 (fps) | 17 | 34 | 76 |

| Resource Utilization (LUT4) | | | |
|---|---|---|---|
| MPF100 LEs | 25% | 43% | |
| MPF200 LEs | 14% | 24% | 32% |
| MPF300 LEs | 9% | 16% | 21% |
| MPF500 LEs | 6% | 10% | 13% |

| | | | |
|---|---|---|---|
| Fabric Clock | 153 MHz | 143 MHz | 129 MHz |




Configuration Options

Size Configuration: V250, V500, V1000

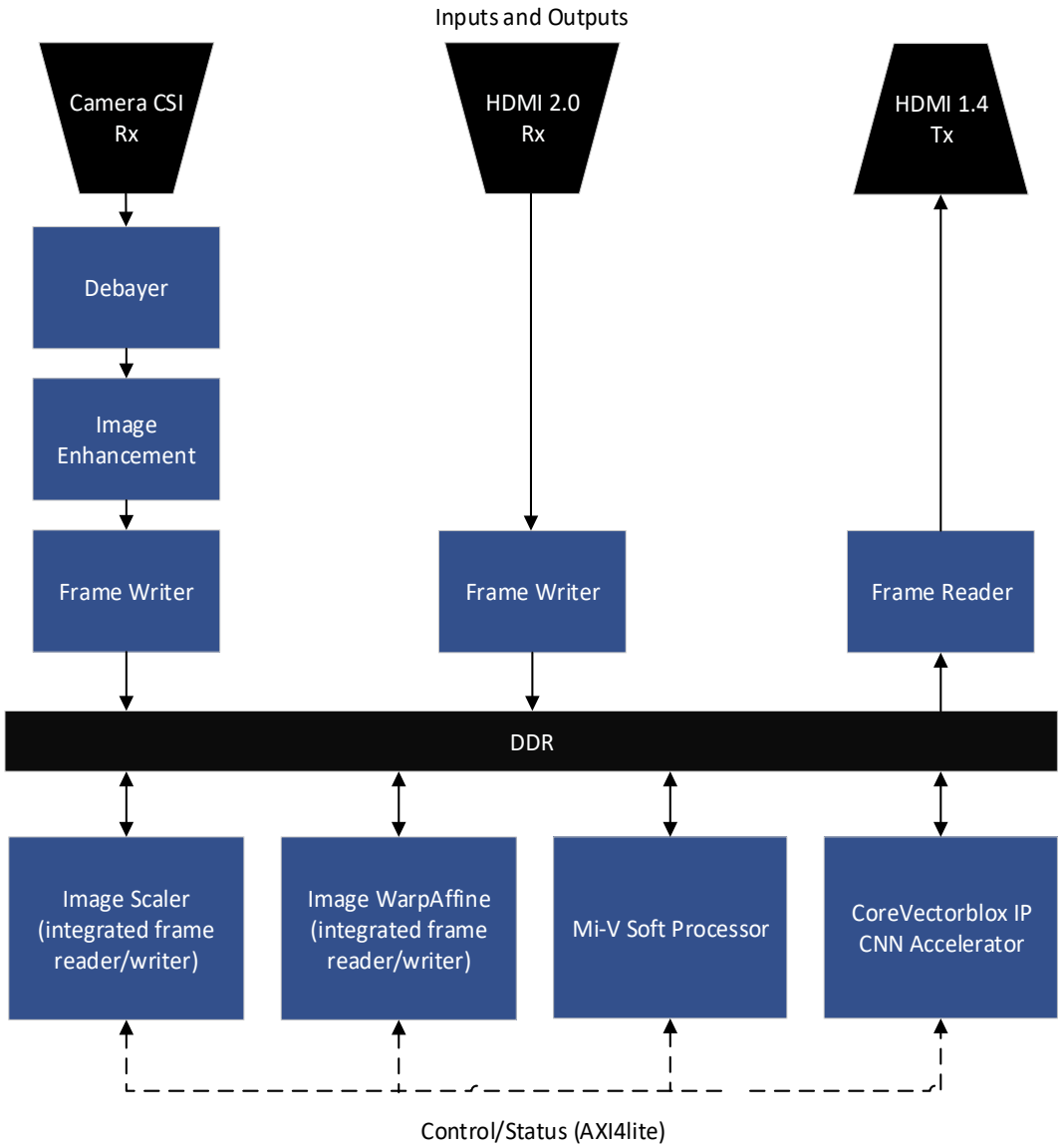
Memory Master Width: 256b, 512b

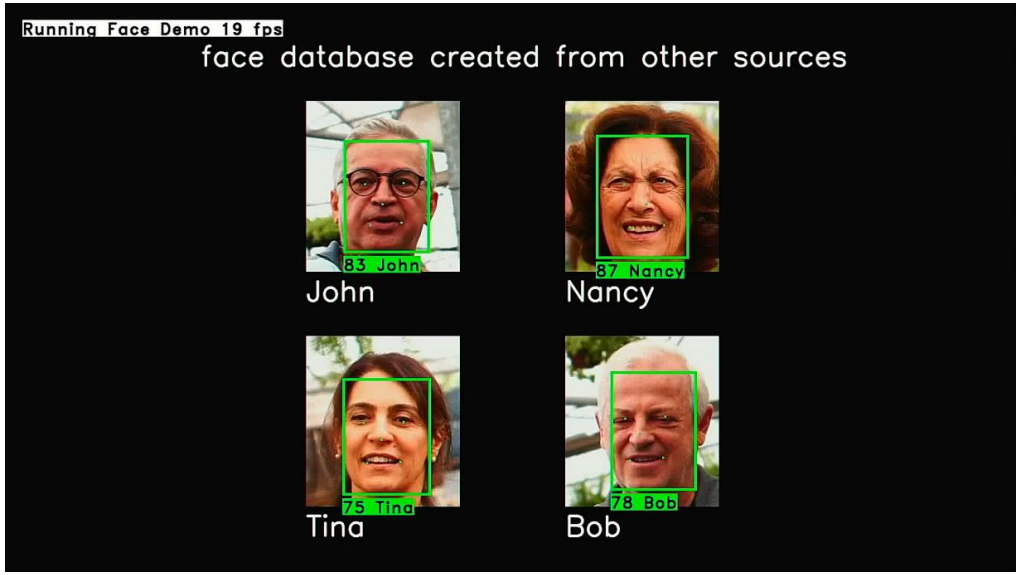
- **Configurable performance based on size and power budget**
- **V2000 (~500 GOPs), V4000 (~750GOPs) are in development***

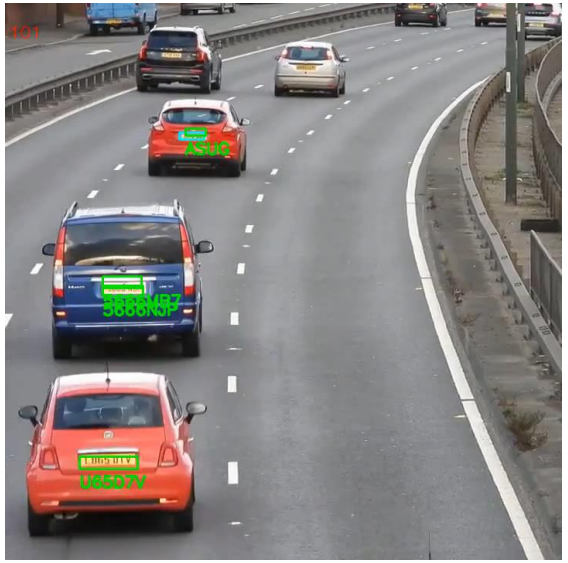
# Facial Recognition Parameters

| | | | |
|---|---|---|---|
| Hardware | MPF300-VIDEO-KIT-NS, Device: MPF300T-1FCG1152E | | |
| Input | HDMI 1080P @60FPS, Center Cropped to 1080x1080 for processing | | |
| Face Detection Model Name | RetinaFace MobileNet | | |
| Face Detection Input Resolution | 320x320 | | |
| Face Detection GOPs | .497 GOPS | | |
| Face Detection Parameters | .423 MParams | | |
| Face Recognition Model | Sphereface | | |
| Face Recognition GOPs | 3.504 GFLOPs | | |
| Face Recognition Parameters | 22.671 MParams | | |
| Recognition Database | 5 faces | | |
| Core Vectorblox Configuration | V1000 (MPF200) | V500 (MPF200) | V250 (MPF200) |
| FPGA Resources Total LUT/FF/DSP/uSRAM/LSRAM | 160K/153K/353/1061/507 | 145K/132K/225/837/443 | 128K/112K/145/726/406 |
| FPGA Resources CoreVectorblox LUT/FF/DSP/uSRAM/LSRAM | 60K/69K/292/531/148 | 45K/48K/164/307/84 | 26K/28K/84/16/47 |
| Face Detection Network Runtime | 12 ms | 15 ms | 26 ms |
| Face Recognition Network Runtime | 31 ms | 50 ms | 95 ms |
| Total FPS including Post Processing | 15 FPS (67 ms) | 11 FPS (90ms) | 7 FPS (142 ms) |

# VectorBlox v1.3



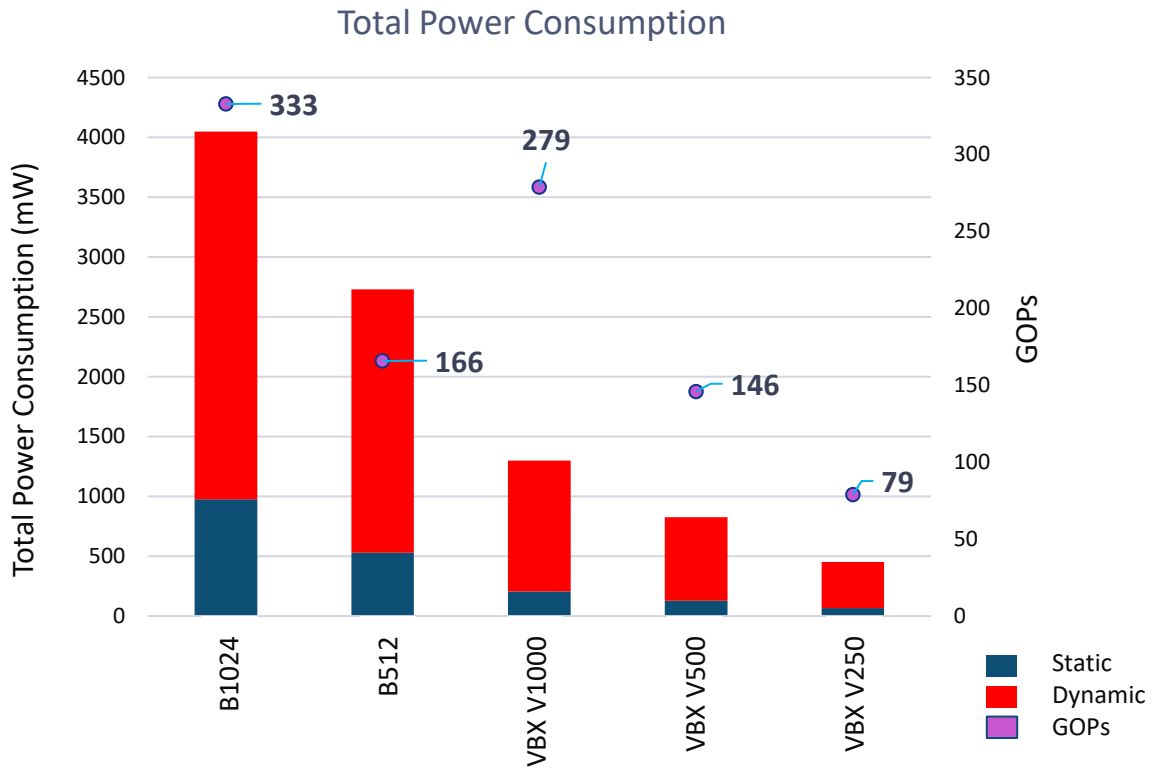



Simulation

# 2-3x More Power Efficient Inference

| Core Name | Peak GOPs | Dynamic Power (mW) | Static Power* (mW) | Total Power (mW) | Total Power (mW/GOP) |
|---|---|---|---|---|---|
| VectorBlox V1000 | 279 | 1094 | 206 | 1300 | **5.1** |
| VectorBlox V500 | 146 | 698 | 127 | 825 | 6.4 |
| VectorBlox V250 | 79 | 387 | 65 | 452 | 7.1 |
| Comp A B1024 | 332.8 | 3072 | 976 | 4048 | 12.2 |
| Comp A B512 | 166.4 | 2201 | 528 | 2729 | 16.4 |




- **2-3x more power efficient inferencing for similar performance output**
- **Suitable for applications requiring**
  - Low power consumption, small enclosures and fan less designs

*Scaled for resource utilization

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# VectorBlox Releases

- **v1.0 – Nov 2020**
  - VectorBlox SDK
  - CoreVectorBlox V250, V500, and V1000
  - Video kit demo
- **v1.1 – Apr 2021**
  - CoreVectorBlox 10% performance gain, 25% size reduction
  - Import directly from DarkNet (YOLO models)
  - More tutorials
- **v1.2 – Oct 2021**
  - HDMI input
  - Face recognition demo
  - Improved quantization algorithm, enabling more models
  - More tutorials
- **V1.3 – May 2022**
  - Improve SDK interface
  - Improve demo camera experience
  - Support new popular models (e.g. YOLOv4)
  - Engine optimizations

# Thank You

# Appendix

# Useful Links

- ***Smart Embedded Vision Webpage:***

  *https://www.microchip.com/en-us/solutions/industrial/smart-embedded-vision*
- ***Kit Webpage:***
  - *https://www.microchip.com/en-us/development-tool/MPF300-VIDEO-KIT-NS*

# PolarFire DirectCores Included in Libero

| Bus Interface | Memory | Processor/ Controller | Security | DSP | Communication | Peripheral |
|---|---|---|---|---|---|---|
| CoreAXI4Interconnect | PF_SRAM_AHBL_AXI (Configurator) | CoreABC | Crypto (Configurator) | CoreDDS (NCO) | CoreJESD204BRX | CorePCS |
| CoreAHBL2AHBL Bridge | DPLSRAM (Configurator) | CoreRISCV_AXI4 | Tamper(Configurator) | CoreFIR_PF | CoreJESD204BTX | CoreUART |
| CoreAHBLite | CoreFIFO | CoreCortex M1 | | CoreLNSQRT | CoreRSDEC | CoreUART_APB |
| CoreAHBLTOAXI | DDR3 (Configurator) | CoreJTAGDebug | | CoreFPU | CoreRSENC | CoreGPIO |
| CoreAHBtoAPB3 | DDR4 (Configurator) | MiV_RV32IMAF_L1_AHB | | | CorePWM | CoreI2C |
| CoreAPB3 | PolarFire SRAM (Configurator) | MiV_RV32IMA_L1_AHB | | | LiteFast (Obfuscated) | CoreMDIO_APB |
| CoreAXItoAHBL | LPDDR3 (configurator) | CoreBootStrap | | | CoreEDAC | CoreSPI |
| CoreAXI4SRAM | PF_QDR (Configurator) | | | | CPRI v6.1 | CoreRMII |
| | CoreMMC | | | | Complex Multiplier | CoreTimer |
| | | | | | TCAM | CoreAXI4DMAController |
| | | | | | | PF_System_Services |
| | | | | | | CoreLSM |
| | | | | | | CoreReset_PF |
| | | | | | | CoreSmartBERT |
| | | | | | | CoreMMC |

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# PolarFire Paid DirectCores

| Core Name | Obfuscated | RTL |
|---|---|---|
| Core429/Core429_APB | $20,000 | $50,000 |
| CoreSGMII | $500 | Sibridge (microsemi.sales@sibridge.com) |
| CoreTSE/ CoreTSE_AHB | $4,000 | Sibridge (microsemi.sales@sibridge.com) |
| CorePCIF/ CorePCIF_AHB | $20,000 | $50,000 |
| CoreFFT | N/A | $5,500 |
| CoreCIC | N/A | $3,000 |
| 10GBASE-R (Core10GMAC) | $10,000 | N/A |
| 10GBASE-KR (Core10GMAC)<br>Only 32-bit Implementation | $10,000 | N/A |
| CoreXAUI (XAUI, RXAUI) | Free | $25000 |
| CoreQSGMII | $2,000 | NA |
| CoreSDIRx/Tx (SD/HD/3G) | Freely available with Libero Gold and Platinum License | NA |